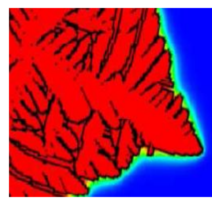
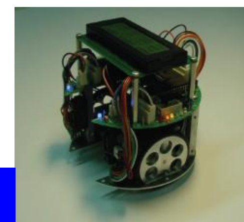
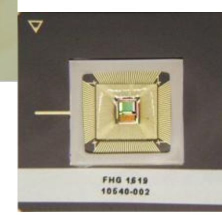
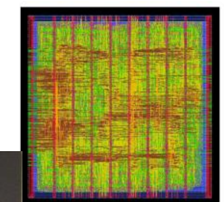
More than the Machine –
Using Memristors for Computing





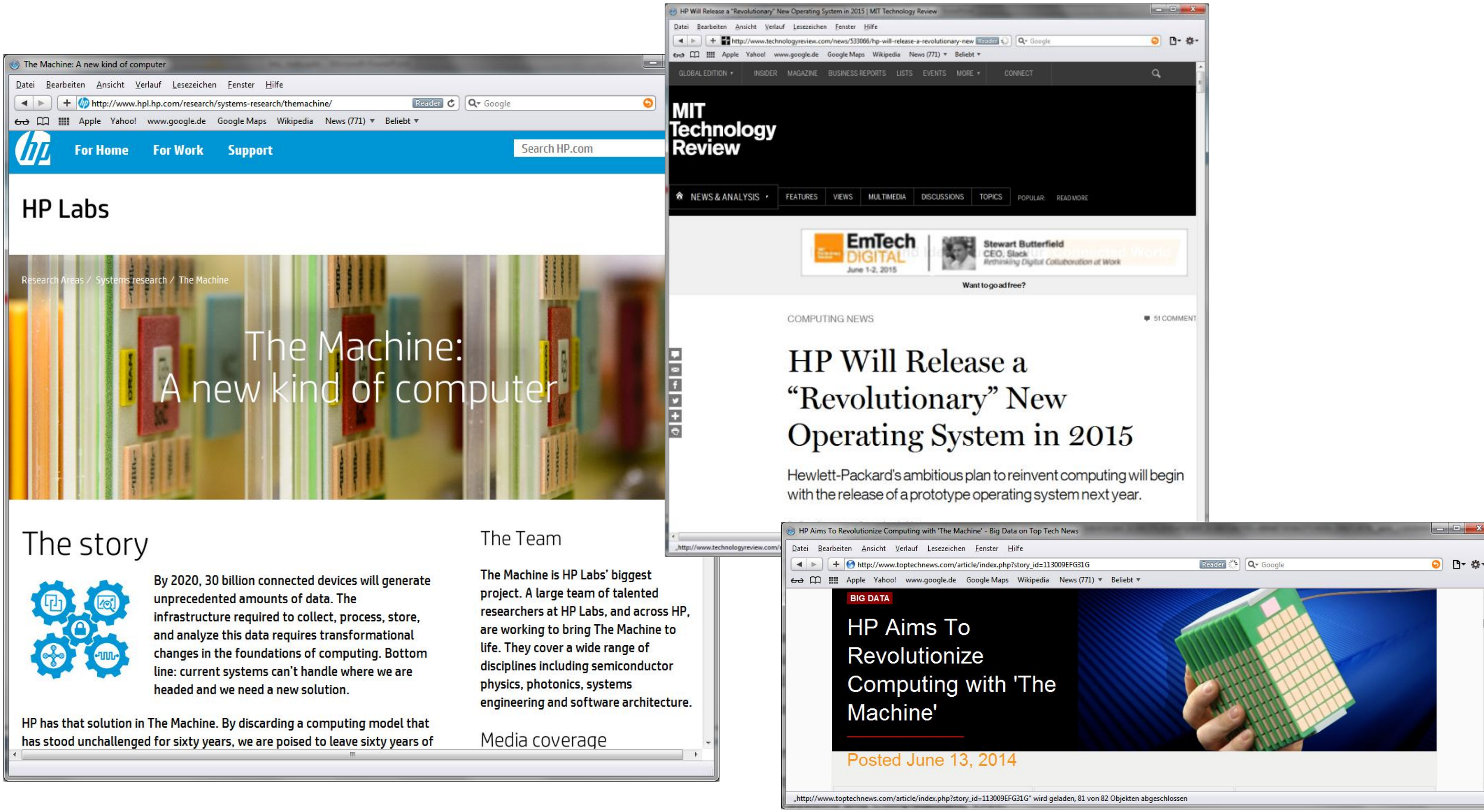




Dietmar Fey
Department Computer Science –
Chair for Computer Architecture
Friedrich-Alexander-University Erlangen-Nürnberg

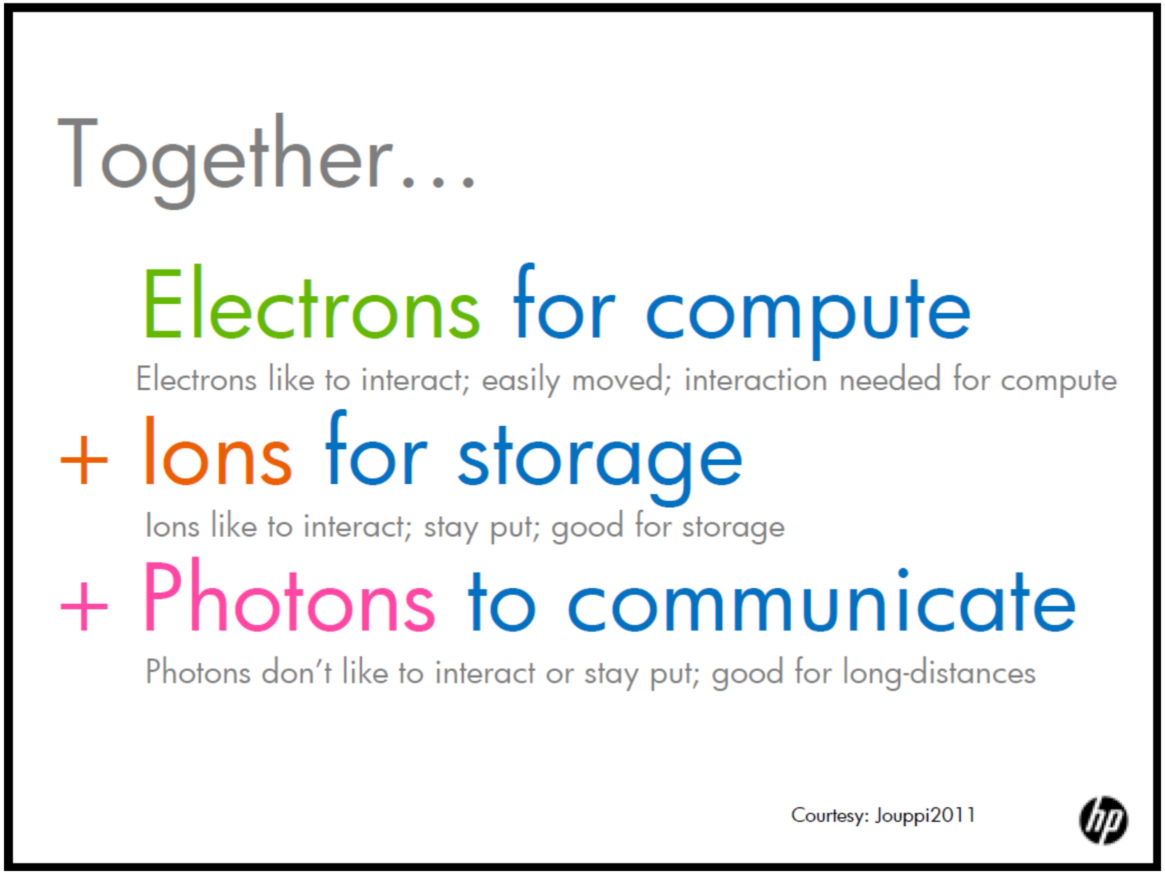
What is the Machine?

- Who is aware of HP's Machine?



What is the Machine?

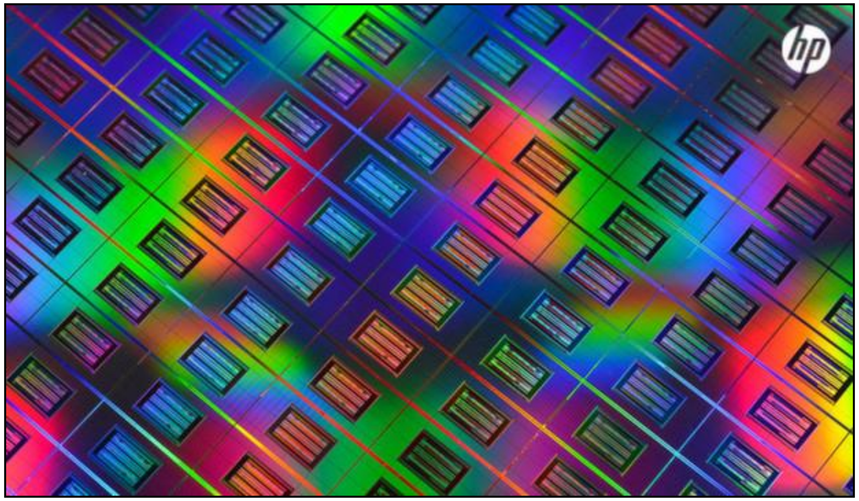
- Utilisation of different technologies



Source: P. Ranganathan, "Saving the world together, one server at a time…" ACACES 2011

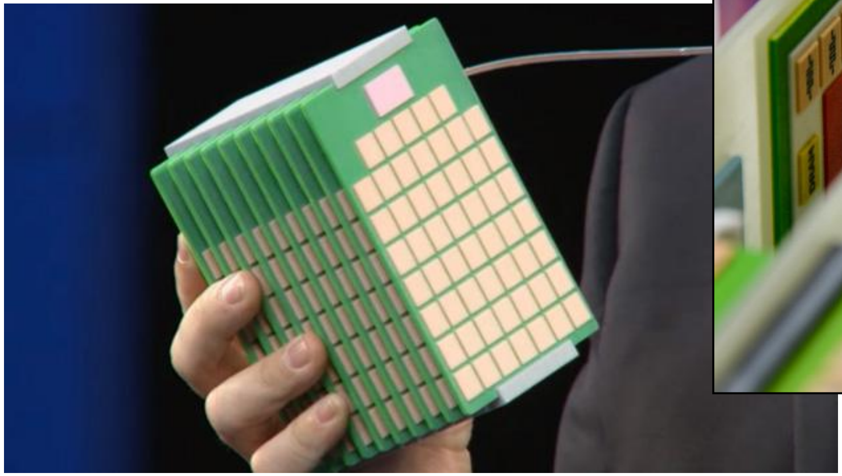
What is the Machine?

- Special purpose cores arbitrarily connected with pool of non-volatile memories – the memristors
  - Access times between 0.3 and 3 ns (< below 250 ns)
  - Mostly flat memory model
    - Paging and TLBs shall become obsolete
    - Vision: Cache becomes non-volatile



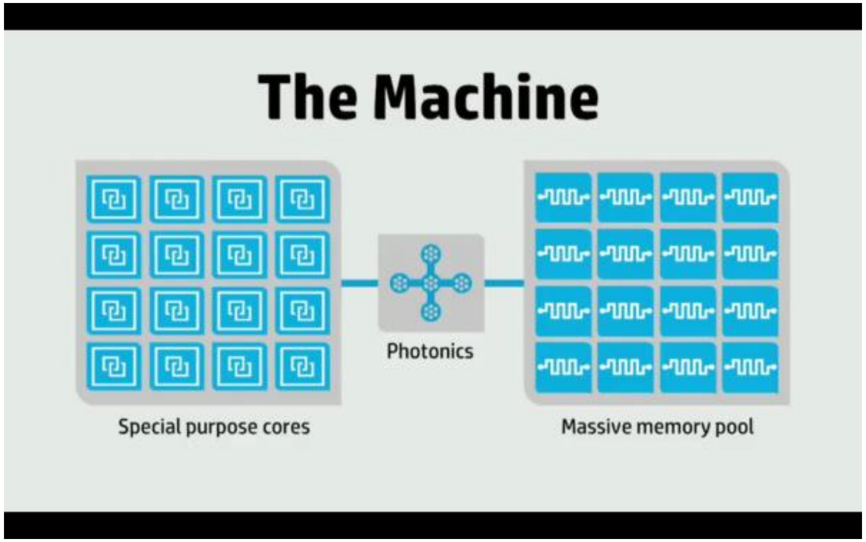
What is the Machine?

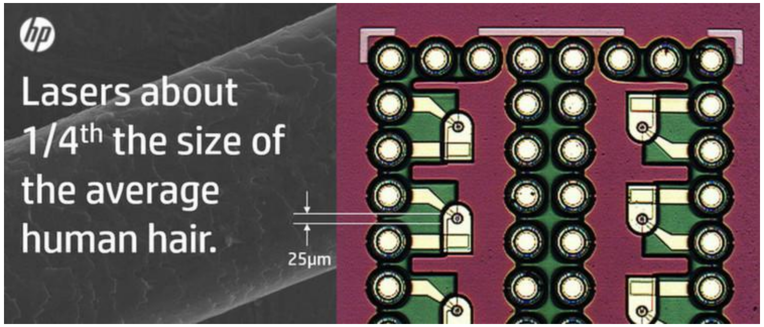
- What is the Machine?
  - HP will provide first products of a complete new computer architecture within the next two to three years
  - Up 160 racks based on memristors connected to a cluster
    - Data capacity up to 160 Petabyte
    - Size of a refrigerator



What is the Machine?

- Processor cores and memory connected via high speed fiber optics
  - Bandwidth of 6 Terabit / second

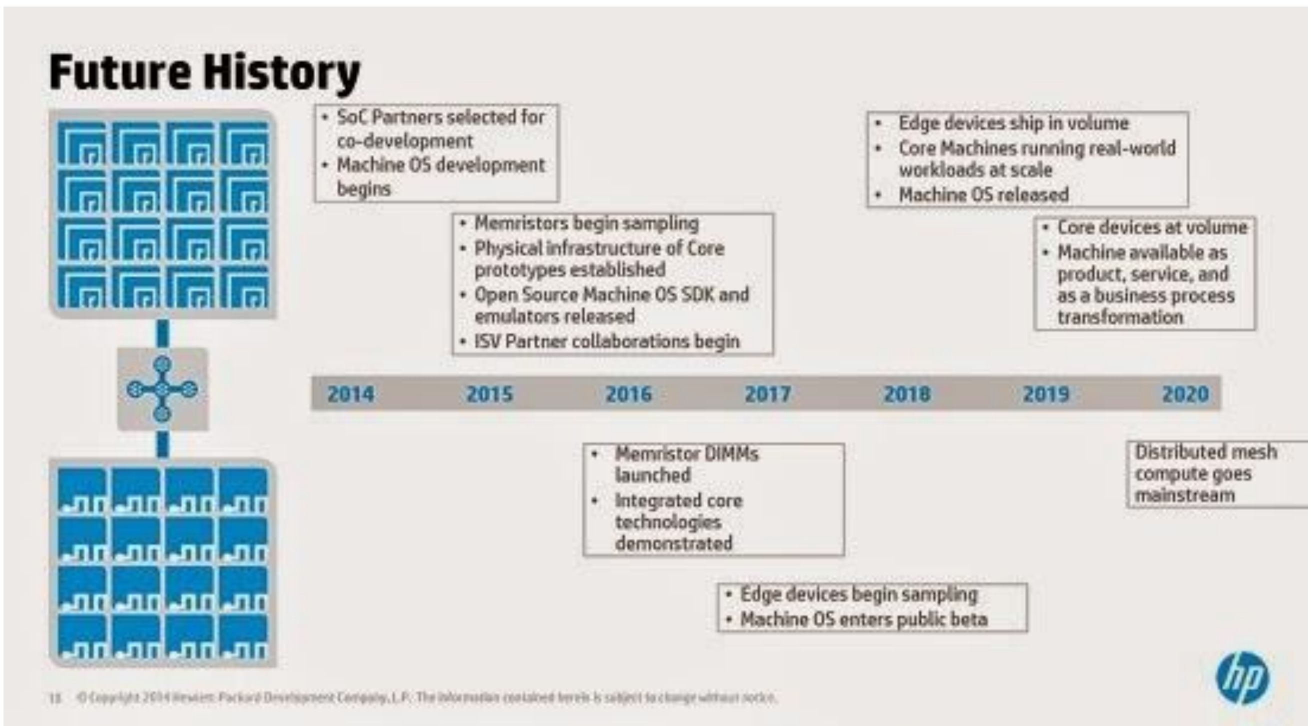




- Machine rack no server
  - Architecture flexible configurable from mobile device up to large computer

What is the Machine?

- Schedule for the revolution
  - New memory controllers
  - New OS for the Machine: Linux++ → Carbon

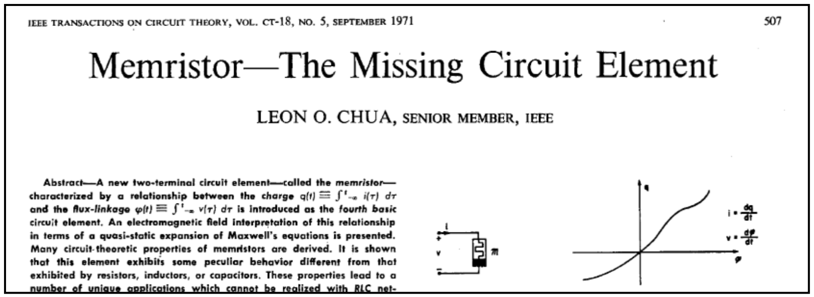


Outline

- What is the Machine?
- Memristor technology
- Digital Boolean logic with memristors
- Ternary Computing using memristors
- Conclusion

Memristor technology

- Memristor - The missing 4th element
  - Predicated by Leon Chua in 1971

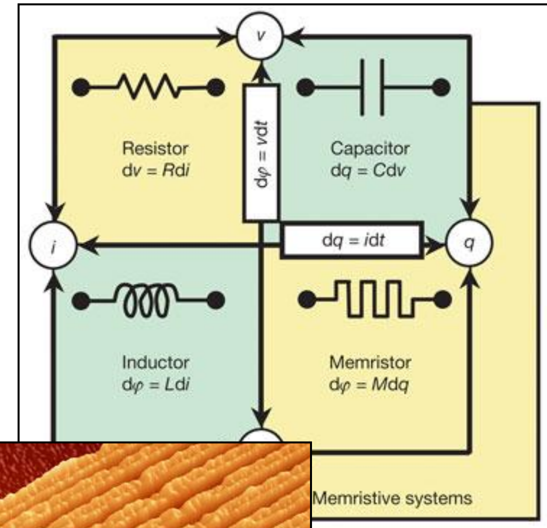


IEEE TRANSACTIONS ON CIRCUIT THEORY, VOL. CT-18, NO. 5, SEPTEMBER 1971 507

Memristor—The Missing Circuit Element

LEON O. CHUA, SENIOR MEMBER, IEEE

Abstract—A new two-terminal circuit element—called the *memristor*—characterized by a relationship between the *charge* $q(t) \equiv \int_{-\infty}^{t} i(\tau)\, d\tau$ and the *flux-linkage* $\varphi(t) \equiv \int_{-\infty}^{t} v(\tau)\, d\tau$ is introduced as the *fourth basic* circuit element. An electromagnetic field interpretation of this relationship in terms of a quasi-static expansion of Maxwell's equations is presented. Many circuit-theoretic properties of memristors are derived. It is shown that this element exhibits some peculiar behavior different from that exhibited by resistors, inductors, or capacitors. These properties lead to a number of unique applications which cannot be realized with *RLC* net-



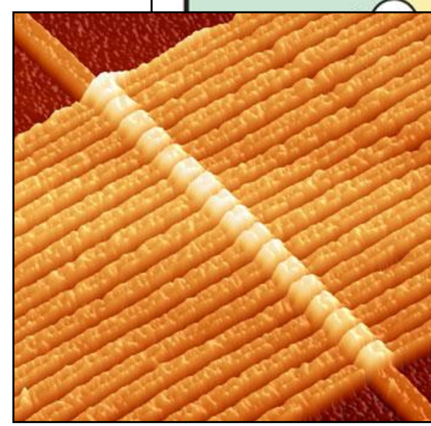
  - Experimentally found in 2008 at HP Lab

nature Vol 453 | 1 May 2008 | doi:10.1038/nature06932

LETTERS

The missing memristor found

Dmitri B. Strukov[1], Gregory S. Snider[1], Duncan R. Stewart[1] & R. Stanley Williams[1]



Memristor technology

- Two principal kinds of memristors
  - Change resistivity of the device, e.g. due to ion transfer

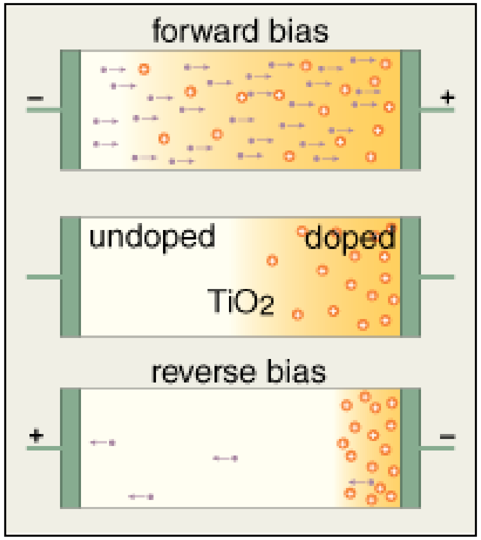
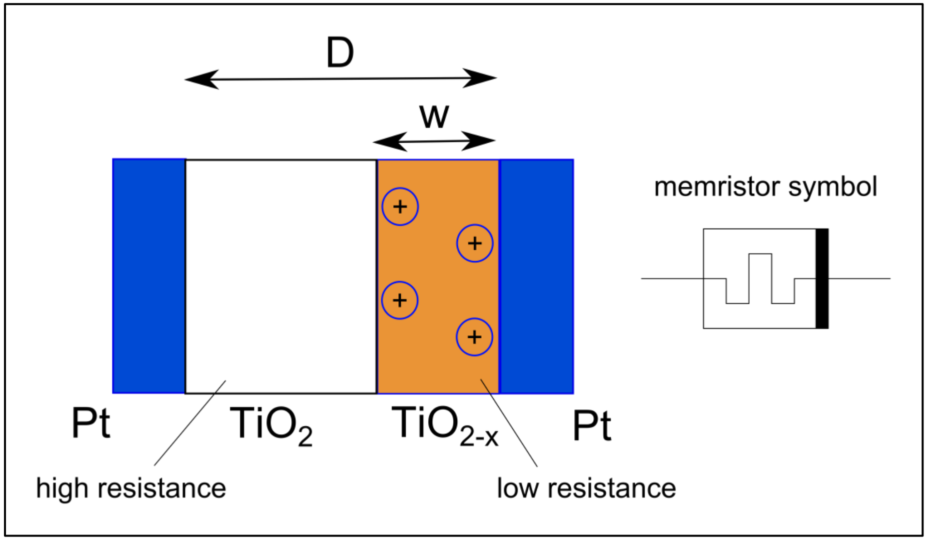


Image from http://bit-player.org/2012/remember-the-memristor

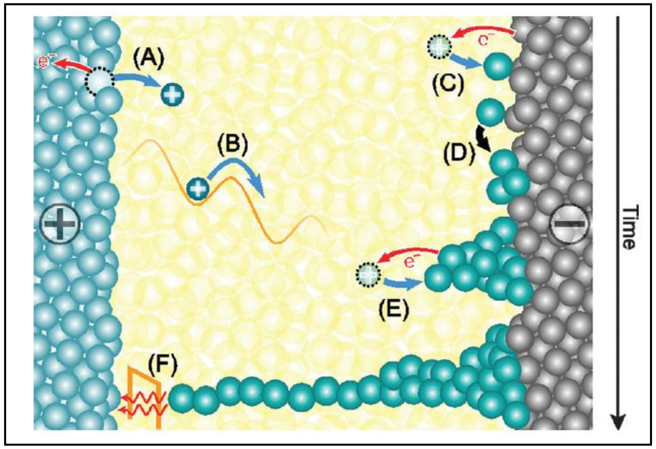


Total memristance = sum of resistances of the doped und undoped regions

$$R_{MEM}(x) = R_{ON} \cdot x + R_{OFF} \cdot (1 - x),$$
$$where \;\; x = \frac{w}{D} \;\; \epsilon \;\; (0, 1)$$

Memristor technology

- ResitiveRAM (ReRAM):
  Growing of a conducting filament due to depositions of cations



Images and equations taken from

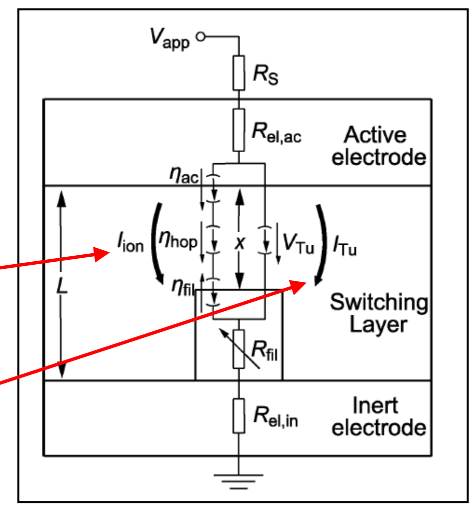
PCCP RSCPublishing

PAPER View Article Online View Journal

Cite this: DOI: 10.1039/c3cp50738f

Switching kinetics of electrochemical metallization memory cells

Stephan Menzel,*[a] Stefan Tappertzhofen,[b] Rainer Waser[ab] and Ilia Valov*[a]



- More complicated model than to the HP model before

$$I_{\mathrm{fil,SET}} = j_{0,\mathrm{et}} A_{\mathrm{fil}} \left(\exp\left(-\frac{\alpha e z}{k_B T} \eta_{\mathrm{fil}} \right) - 1 \right)$$

$$I_{\mathrm{Tu}} = C \frac{3\sqrt{2 m_{\mathrm{eff}} \Delta W_0}}{2x} \left(\frac{e}{h}\right)^2 \exp\left(-\frac{4\pi x}{h} \sqrt{2 m_{\mathrm{eff}} \Delta W_0} \right) A_{\mathrm{fil}} V_{\mathrm{Tu}}.$$

- Modelling memristor behaviour

Zdeněk BIOLEK, Dalibor BIOLEK Viera BIOLKOVÁ
SPICE Model of Memristor with Nonlinear Dopant Drift
RADIOENGINEERING, VOL. 18, NO. 2, JUNE 2009

  - Used in a SPICE simulation

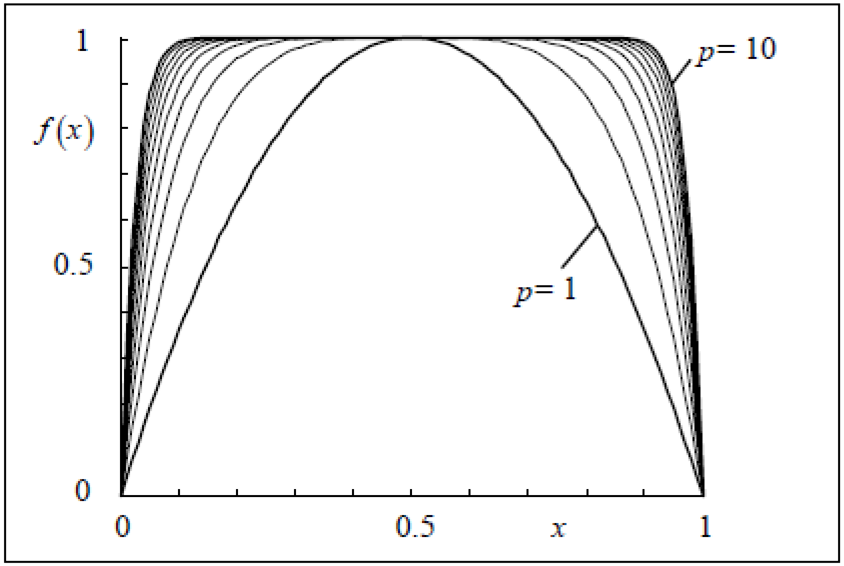
$$\frac{dx}{dt} = k\, i(t) f(x), \quad k = \frac{\mu_v R_{ON}}{D^2}$$

$$v(t) = R_{MEM}(w)\, i(t).$$

  - Using a model for a non-linear dopant drift (window function)

Used window function

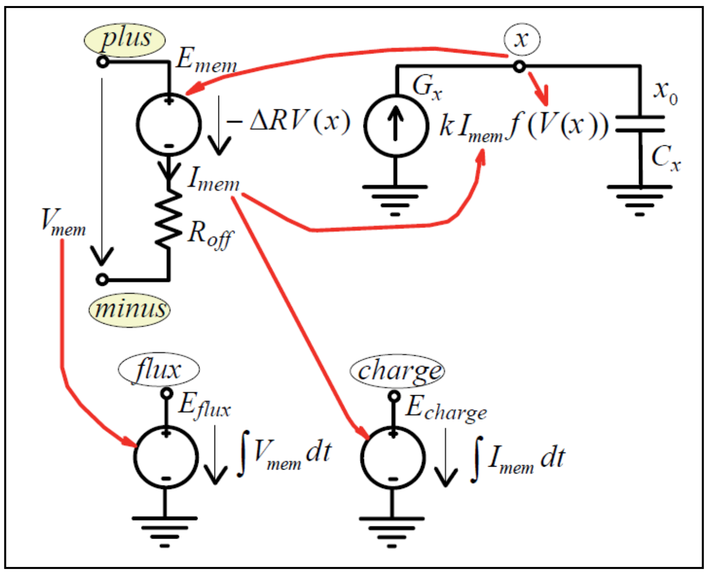
$$f(x) = 1 - (2x-1)^{2p}$$



Memristor technology

- Modelling and simulating memristors
  - Use an equivalent SPICE circuit model
  - Simplifies execution of mixed-signal simulations

Zdeněk BIOLEK, Dalibor BIOLEK Viera BIOLKOVÁ
SPICE Model of Memristor with Nonlinear Dopant Drift
RADIOENGINEERING, VOL. 18, NO. 2, JUNE 2009

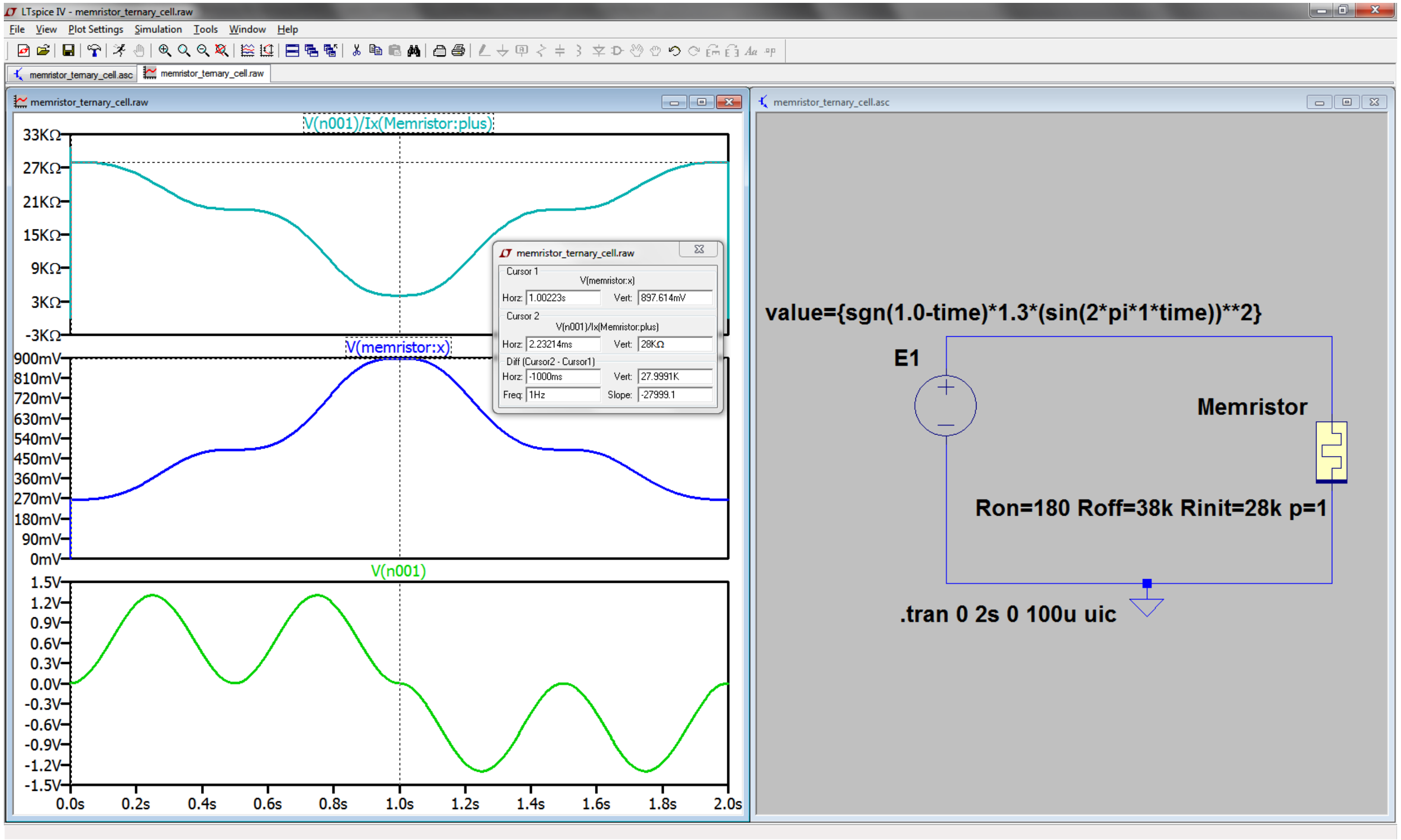



```
* HP Memristor SPICE Model
* For Transient Analysis only
* created by Zdenek and Dalibor Biolek
**************************
* Ron, Roff   - Resistance in ON / OFF States
* Rinit       - Resistance at T=0
* D           - Width of the thin film
* uv          - Migration coefficient
* p           - Parameter of the WINDOW-function
*               for modeling nonlinear boundary conditions
* x           - W/D Ratio, W is the actual width
*                 of the doped area (from 0 to D)
*
.SUBCKT memristor Plus Minus PARAMS:
+ Ron=1K Roff=100K Rinit=80K D=10N uv=10F p=1
**********************************************
* DIFFERENTIAL EQUATION MODELING  *
**********************************************
Gx 0 x value={ I(Emem)*uv*Ron/D^2*f(V(x),p)}
Cx x 0 1 IC={(Roff-Rinit)/(Roff-Ron)}
Raux x 0 1T
```

```
* RESISTIVE PORT OF THE MEMRISTOR *
*******************************
Emem plus aux value={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}
**********************************************
*Flux computation*
**********************************************
Eflux flux 0 value={SDT(V(plus,minus))}
**********************************************
*Charge computation*
**********************************************
Echarge charge 0 value={SDT(I(Emem))}
**********************************************
* WINDOW FUNCTIONS
* FOR NONLINEAR DRIFT MODELING *
**********************************************
*window function, according to Joglekar
.func f(x,p)={1-(2*x-1)^(2*p)}
*proposed window function
;.func f(x,i,p)={1-(x-stp(-i))^(2*p)}
.ENDS memristor
```

Memristor technology

- Modelling multi-bit feature
  - Demonstration in a SPICE simulation

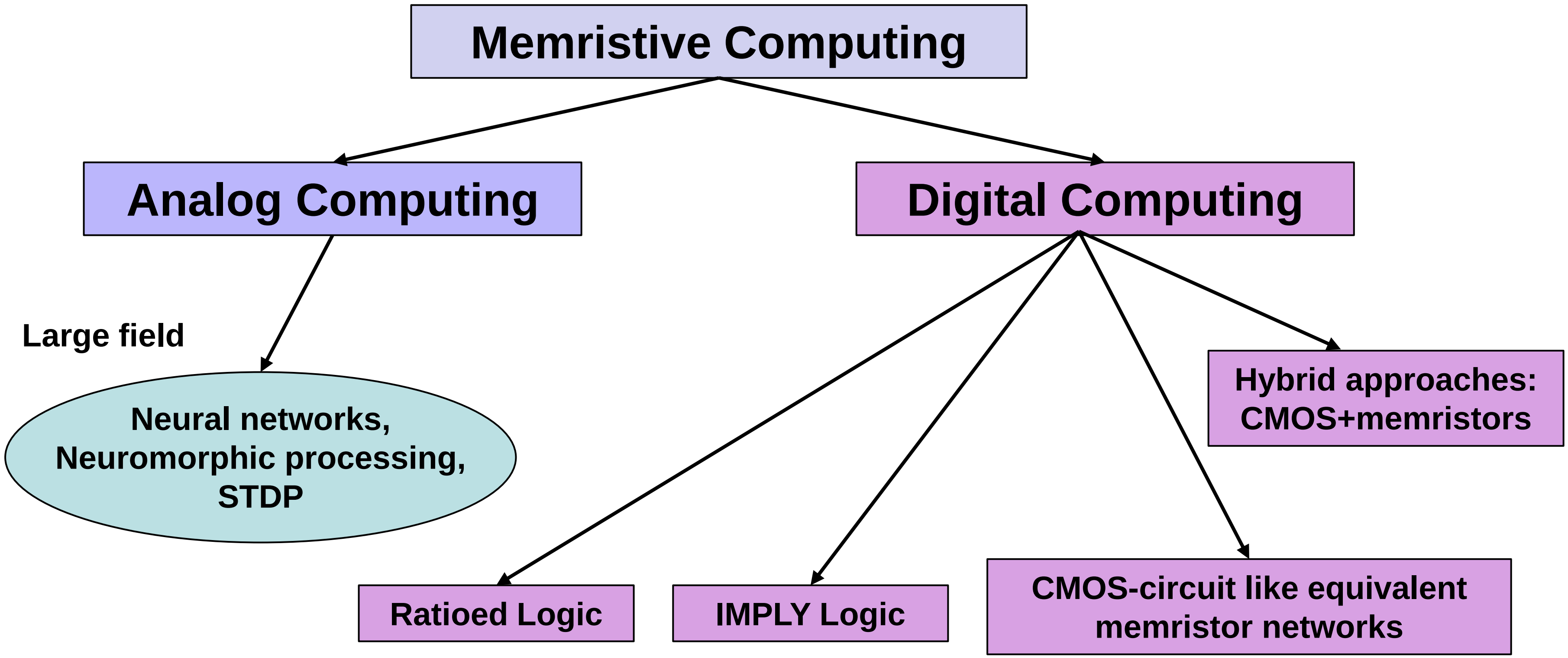


Outline

- What is the Machine?
- Memristor technology
- Digital Boolean logic with memristors
- Ternary Computing using memristors
- Conclusion

Digital Boolean logic with memristors

- Different branches of computing with memristors

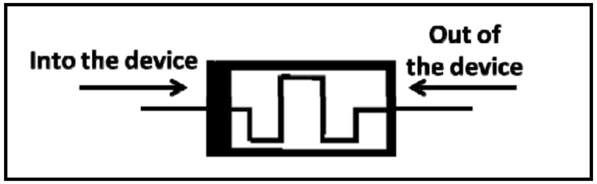


I. Vourkas, G.Ch. Sirakoulis / Memristor-based combinational circuits: A design methodology for encoders/ decoders , Microelectronics Journal 45 (2014) 59–70

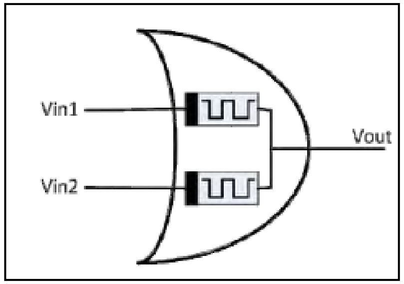
- **Ratioed Logic**

S. KVATINSKY, N. WALD, G. SATAT,
A. KOLODNY, U.C. WEISER, G.E. FRIEDMAN
MRL – Memristor Ratioed Logic
13th International Workshop on CNNA, 1:6, pp. 29-31, 2012.

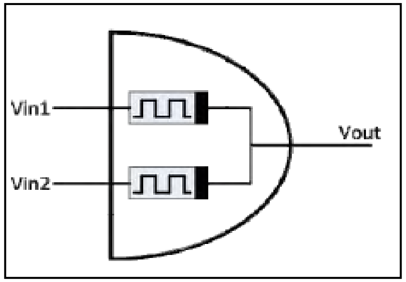
- Creating simple AND- and OR- gates by (mem)resistive networks
- Making following abstraction
  - Current flowing into the device: memristance ↓
  - Current flowing out of the device: memristance ↑



Structure of OR gate



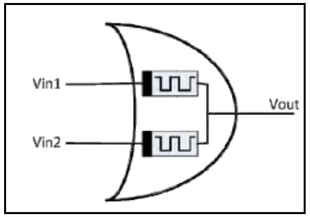
Structure of AND gate



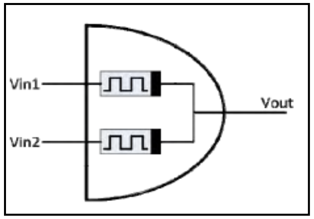
Digital Boolean logic with memristors

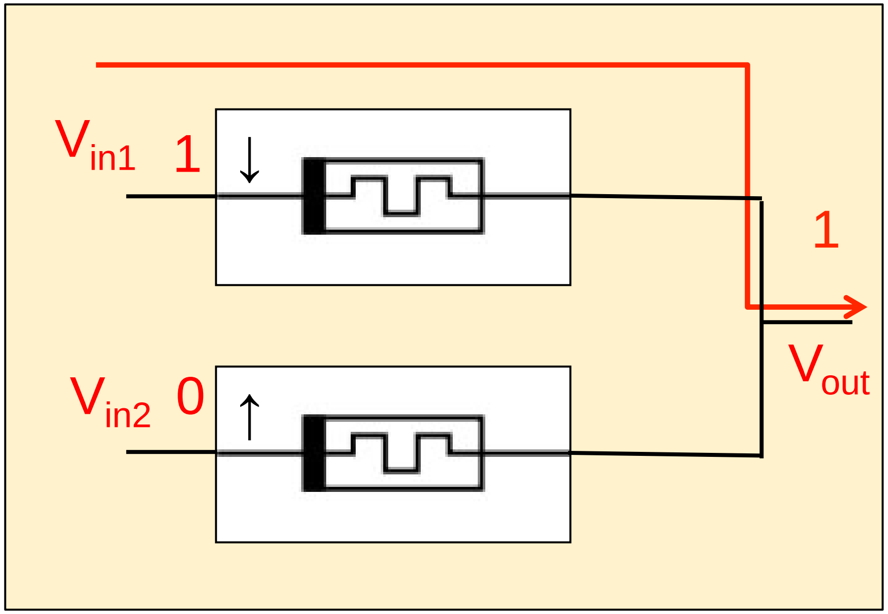
- Example for OR and AND gate for input $V_{in1} = 1$ and $V_{in2} = 0$

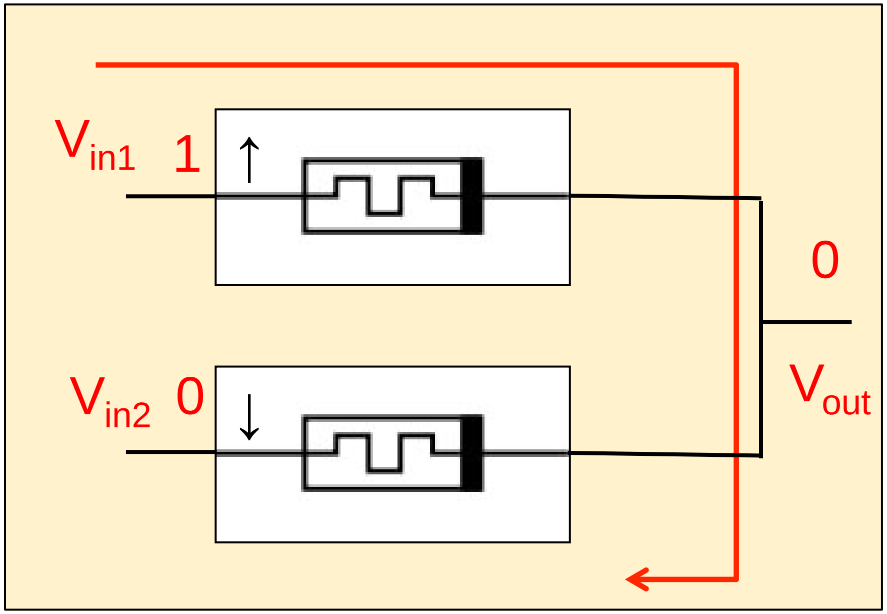
OR gate



AND gate







Digital Boolean logic with memristors

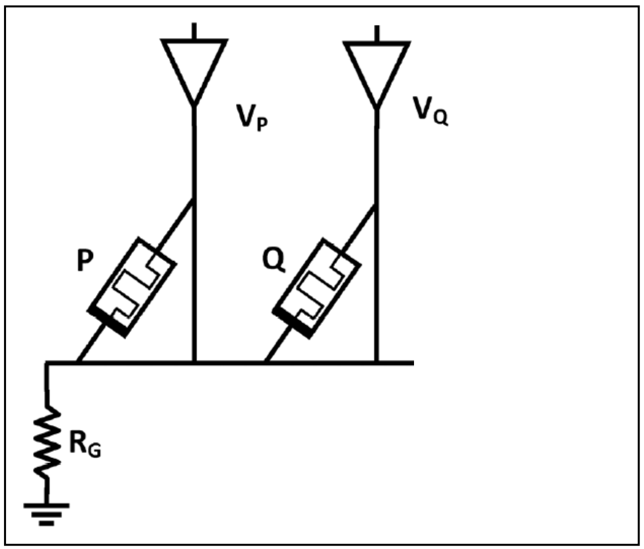
- IMPLY Logic
  - Based on conditional toggling (kind of 3-phase logic)
    - Initializing certain states in memristors by input data
    - Apply constant voltages (V_{cond} and V_{set}) that possibly change states
    - Reading out the state (applying voltage that does not change states)

Vol 464 | 8 April 2010 | doi:10.1038/nature08940 nature

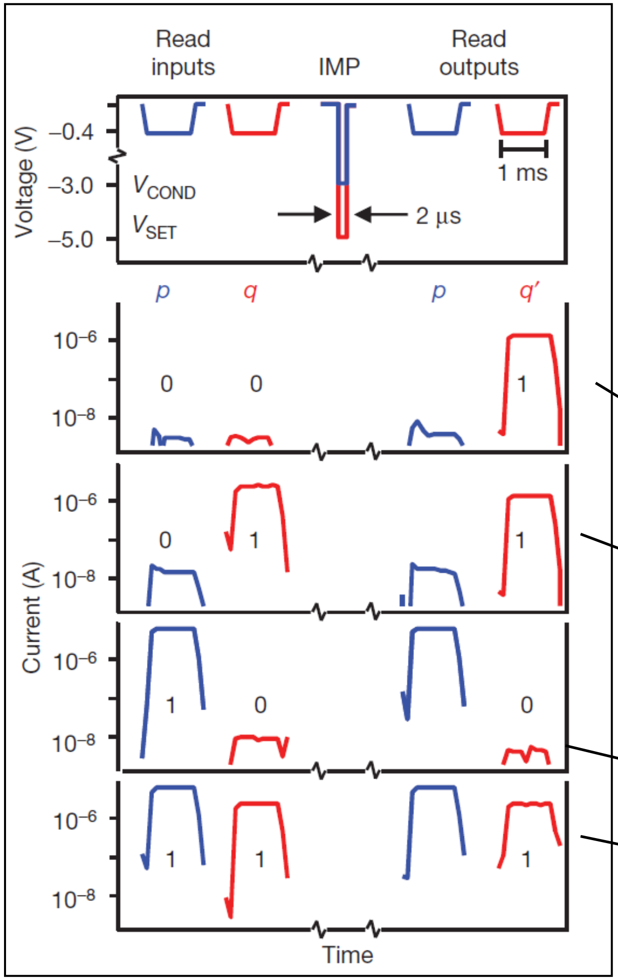
LETTERS

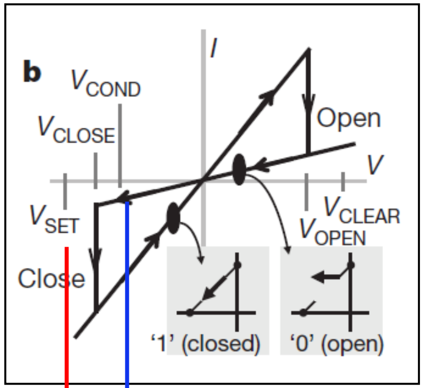
'Memristive' switches enable 'stateful' logic operations via material implication

Julien Borghetti[1], Gregory S. Snider[1], Philip J. Kuekes[1], J. Joshua Yang[1], Duncan R. Stewart[1]† & R. Stanley Williams[1]



- State changing after time

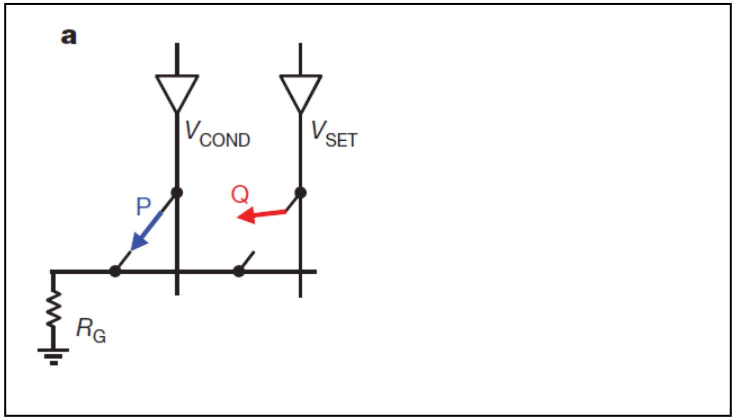




V_{COND} let p‘ ← p

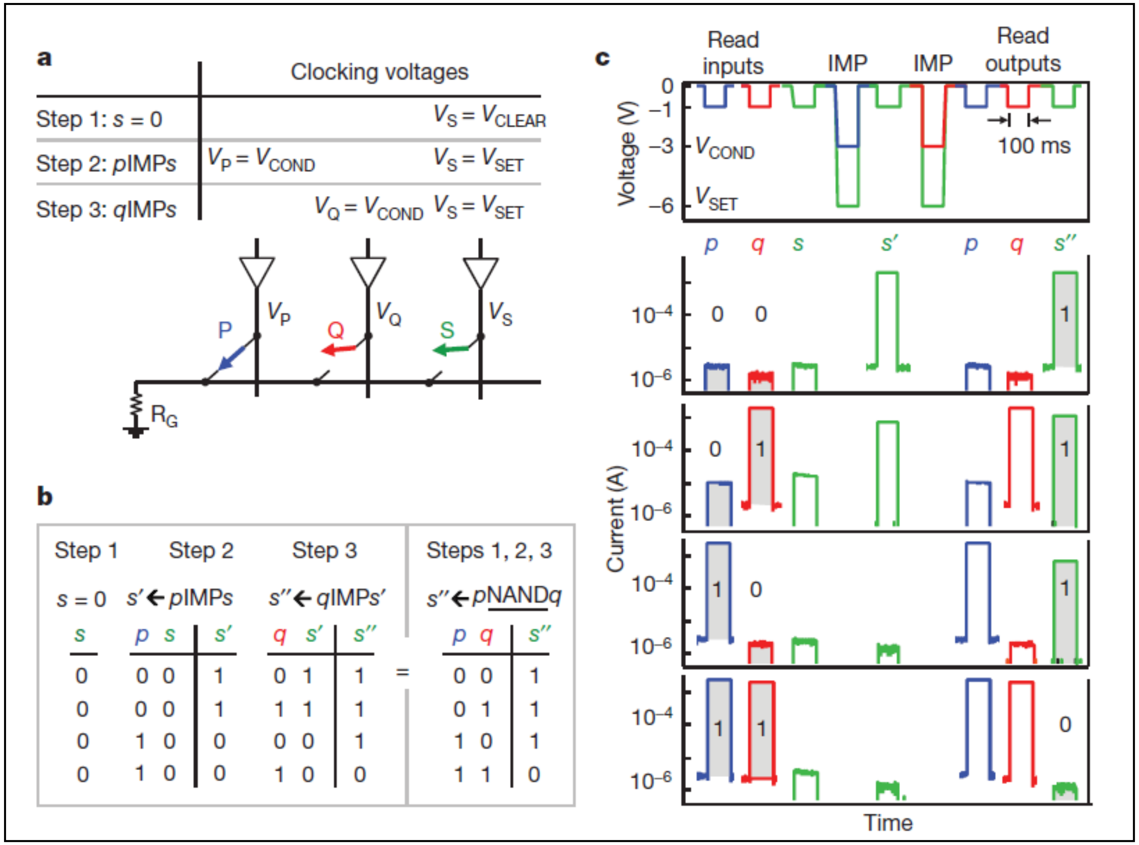
V_{SET} makes q‘ ← 1 if p is opened

Behaviour corresponds exactly to IMPLY logic
p → q = q‘



Digital Boolean logic with memristors

- Can be expanded to NAND by subsequent IMP operations



Outline

- What is the Machine?
- Memristor technology
- Boolean logic with memristors
- Ternary Computing using memristors
- Conclusion

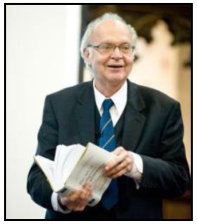
Ternary computing using memristors

- Ternary computers
  - Since the days of Konrad Zuse and John v. Neumann
    - Binary computers
  - Ternary system
    - differentiates between 3 and not 2 states
  - 17th century: Caramuel y Lobkowitz
    - investigated number system with digits 0, 1, and 2

http://ternary.3neko.ru/history_of_ternary.html

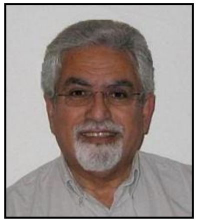
Ternary computing using memristors

- 18th century: Abraham Gotthelf Kästner
  - each number weighted sum of multiples of 3
  - Weights were -1, 0, and +1



- Donald Knuth
  - Denoted that as balanced ternary system

- 1961: Avizienis [IRE Trans. Trans. Electron Computers]
  - Fast carry-free addition with signed-digit (SD) numbers
  - Difficult to implement in digital electronics



- 1988: Parhami
  - Binary SD number system

- 1958: Brousentsov
  - SETUN ternary computer

Ternary computing using memristors

- May be a renaissance of ternary computers?
  - CMOS compatible,
  - fast,
  - Energy-poor,
  - multi-bit storing capable non-volatile memory cells

  like memristors

- Hybrid CMOS-memristor approach

IOP Publishing Semiconductor Science and Technology

Semicond. Sci. Technol. **29** (2014) 104008 (13pp) doi:10.1088/0268-1242/29/10/104008

Using the multi-bit feature of memristors for register files in signed-digit arithmetic units

Dietmar Fey

Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Department Computer Science 3, Chair for Computer Architecture, Martensstr. 3, 91054 Erlangen, Germany

Ternary computing using memristors

- Signed-digit number representation to base 2

$$w(a) = \sum_{i=0}^{n} a_i \cdot 2^i \qquad a = (a_{n-1}, \ldots, a_0),\ \ a_i \in \{-1, 0, 1\}$$

$$\text{Example}: 1\,0\,\bar{1} = 1 \times 2^2 + 0 \times 2^1 - 1 \times 2^0 = 4 - 1 = 3 \qquad ; \bar{1} = -1$$

$$1\,\bar{1}\,1 = 5 - 2 = 3$$

$$0\,1\,1 = 2 + 1 = 3$$

- Used digital coding for signed digits (SD)

a^+	a^-	SD
0	0	0
0	1	-1
1	0	1
1	1	Not used

Ternary computing using memristors

- Carry-free addition in $O(1)$

Binary addition

		1	0	1	1
+		0	1	0	1
C	0	0	0	1	–
S	–	1	1	1	0
C	0	0	1	0	–
S	–	1	1	0	0
C	0	1	0	0	–
S	0	1	0	0	0
S	1	0	0	0	0

$O(n)$
Best case: $log(n)$

Signed digit addition

		1	0	1	1	=	$(11)_{10}$
+		0	1	0	1	=	$(5)_{10}$
C	1	1	1	1	0		
Z	0	$\bar{1}$	$\bar{1}$	$\bar{1}$	0		
S	1	0	0	0	0	=	$(16)_{10}$

$O(1)$

x_i	y_i	z_i	c_{i+1}
0	0	0	0
0	1	-1	1
1	0	-1	1
1	1	0	1

c_i	z_i	s_i
0	0	0
0	-1	-1
1	0	1
1	-1	0

Ternary computing using memristors

- Addition / subtraction of (i) a SD number *a* and a binary number *B* and (ii) two SD numbers *c* and *z*

(i)

$$c_i^+ = a_i^+ \vee \left(B_i \wedge \overline{a_i^-}\right) \qquad \wedge\text{: and} \quad \vee\text{: or}$$

$$z_i^- = \left(a_i^+ \vee a_i^-\right) \oplus B_i \qquad \oplus\text{: exor}$$

(ii)

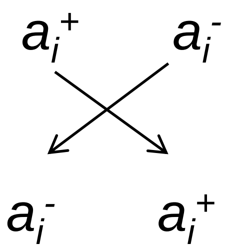
$$s_i^+ = \overline{z_i^-} \wedge c_{i-1}^+$$

$$s_i^- = \overline{c_{i-1}^+} \wedge z_i^-$$

  - *a – B:* Subtraction can be simply reduced to addition

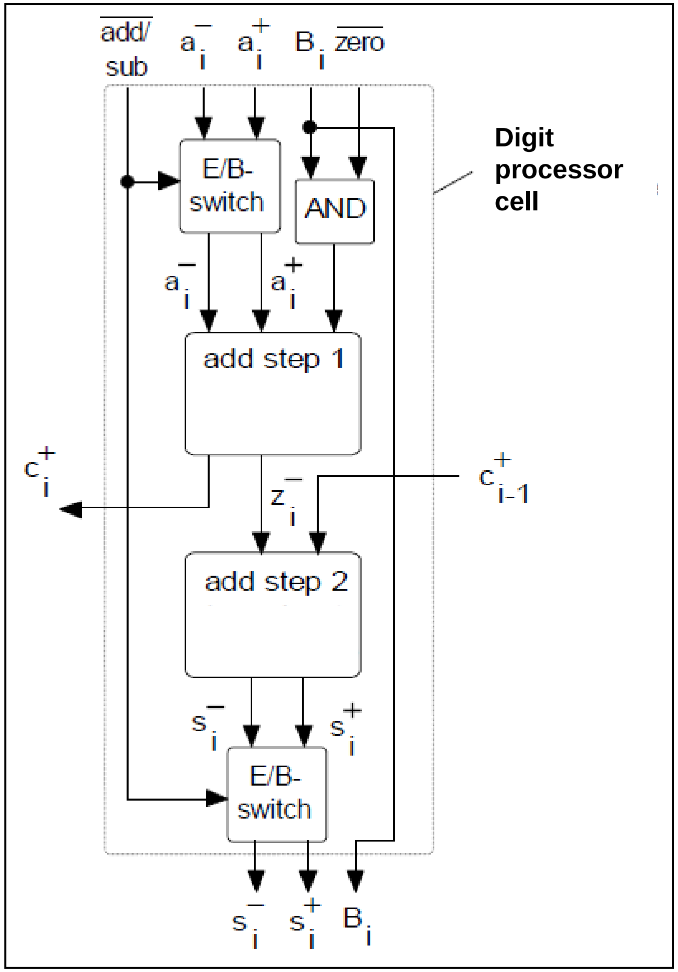
$$a - B = (-1) \cdot \left((-1) \cdot a + B\right)$$

  - Negative complement simply by exchange positive and negative part



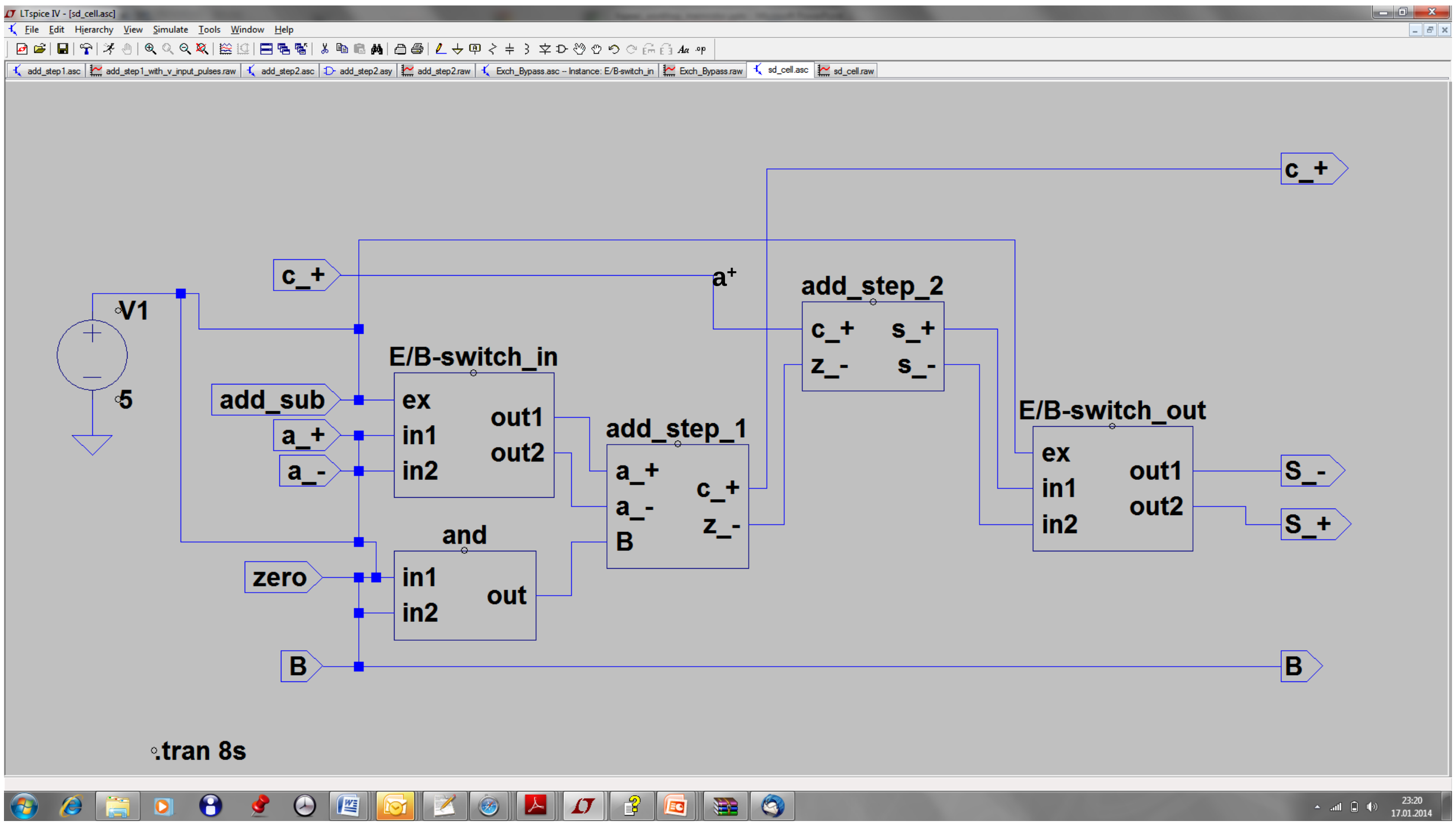
Ternary computing using memristors

- Schematic of a digit processor cell



2 Signed-digit (SD) arithmetic

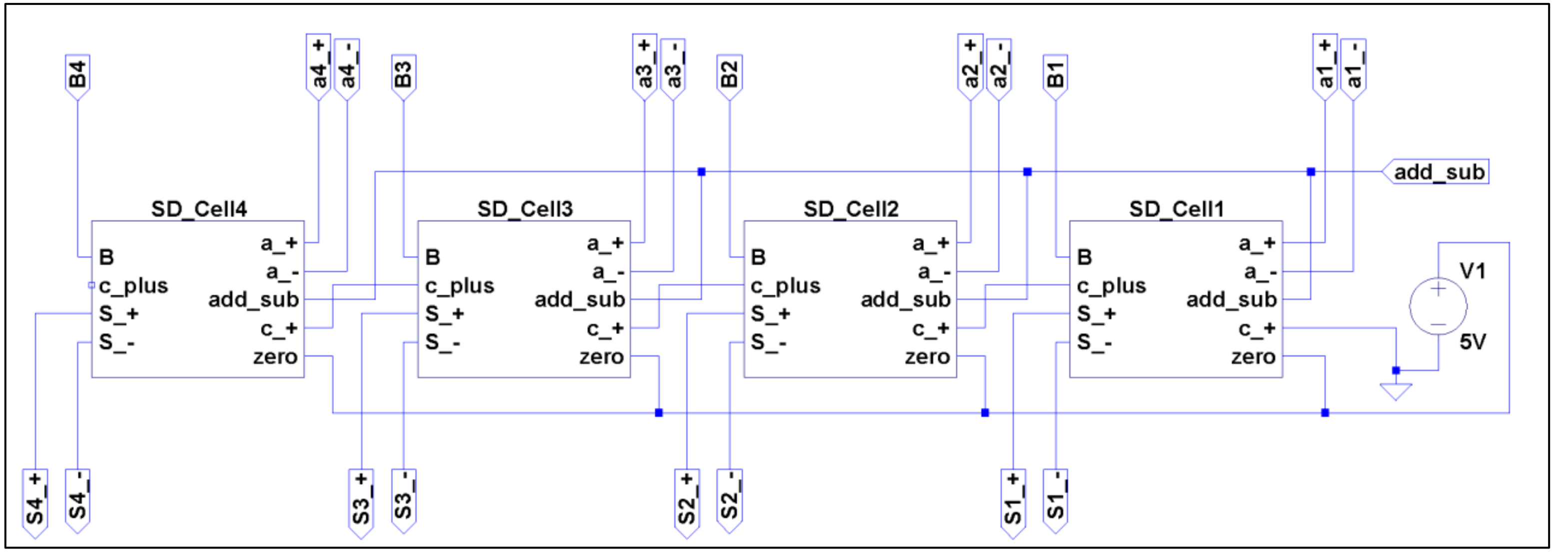
- Corresponding gate logic for an SD adder / subtractor cell
  - Completely implemented in SPICE



Ternary computing using memristors

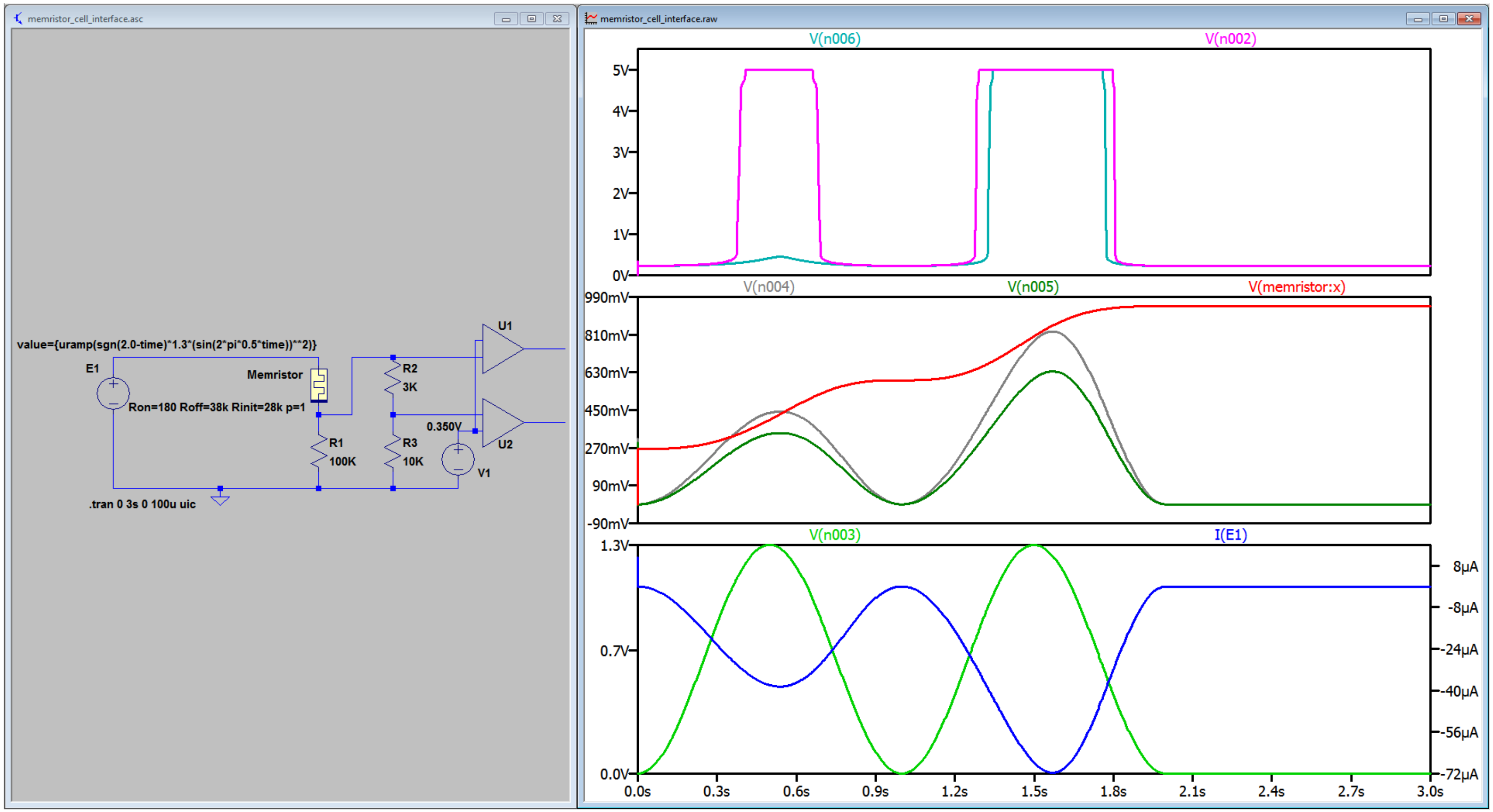
- Schematic of a digit processor cell

  - Several cells are connected side-by-side to a row



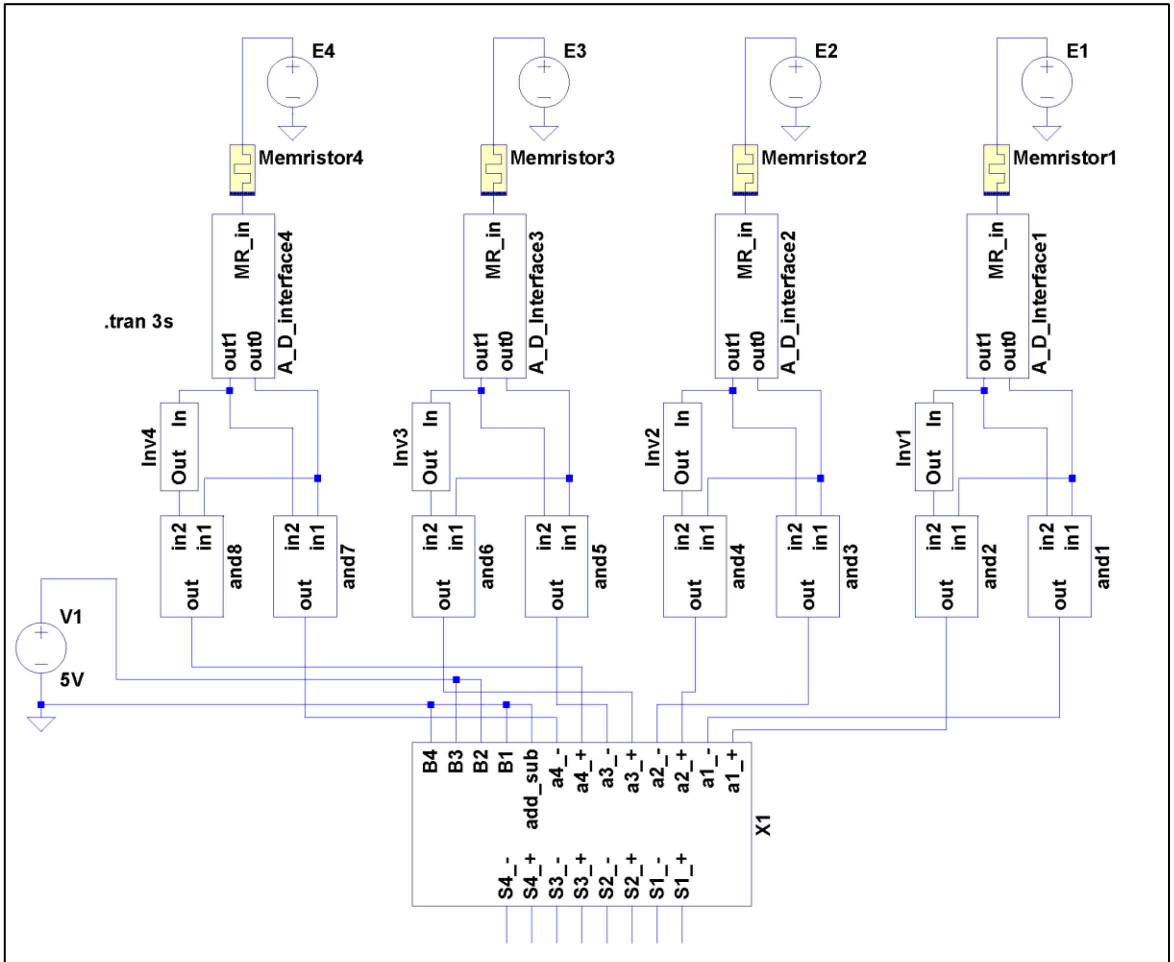
Ternary computing using memristors

- Modelling multi-bit feature
  - Interfacing to produce binary input for digital processing circuit



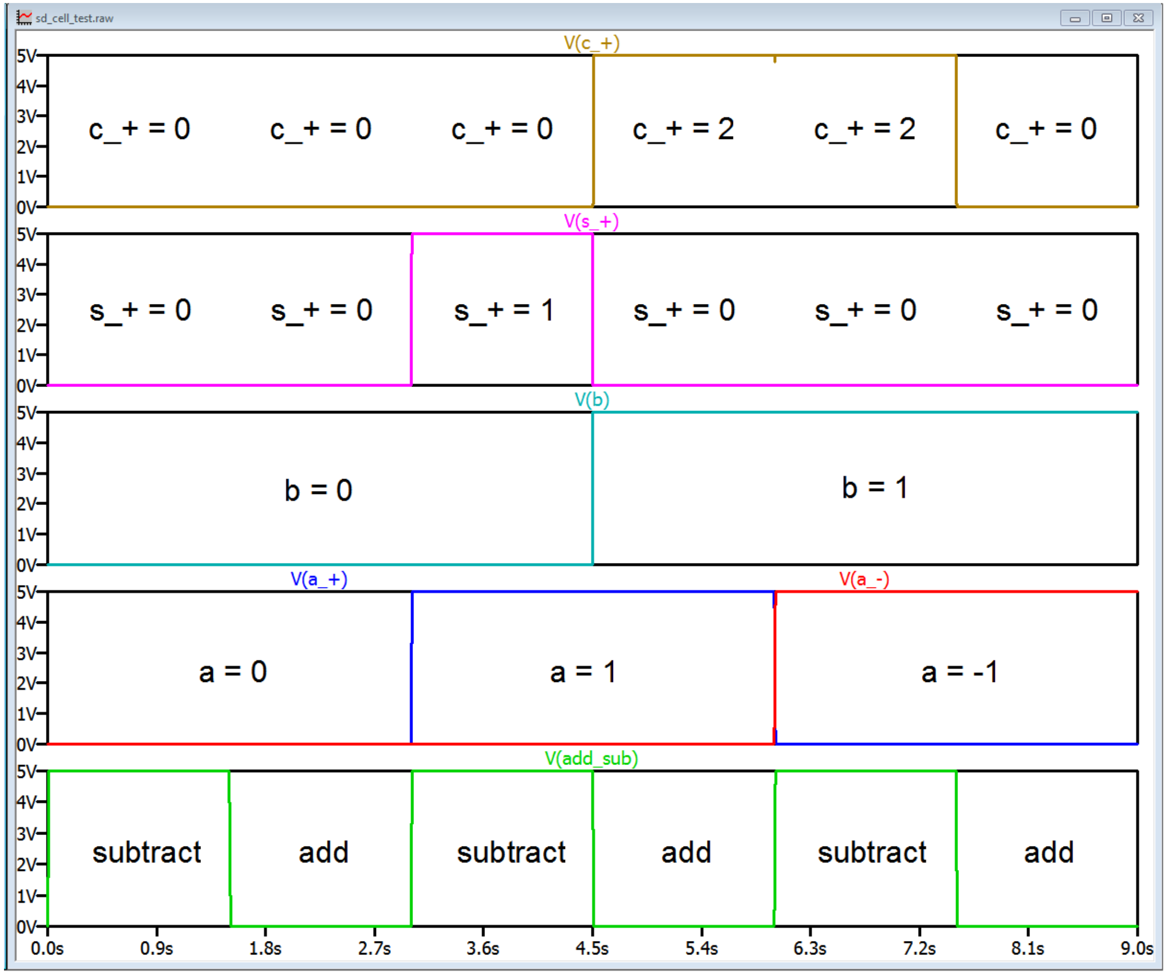
Ternary computing using memristors

- Memristor-based SD arithmetic unit



Ternary computing using memristors

- Simulation result



Conclusion

- Possible computer architecture revolution happens?
- Core technology are NVM like memristors
- Proposal for first memristive Boolean logic gates
- Renaissance or break-through for ternary computers
- Outlook
  - First simple gates have to be realised
  - Devices have to be improved
  - From gates to complex systems