RECENT DEVELOPMENTS IN AUDIOVISUAL QUALITY ASSESSMENT AND MONITORING

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VQEG

Video Quality Experts Group

VIDEO QUALITY EXPERTS GROUP (VQEG)

- **Vision**
  - *"To advance the field of video quality assessment..."*
- **VQEG brings international experts together**
  - Industry
  - Academia
  - Government Organizations
  - ITU – International Telecommunication Union
  - SDO – Other Standard-Developing Organizations
- **VQEG submits reports to SDO, in particular ITU**
- **Selected activities today**
  - Validation of models
  - Development of objective models
  - Improvement of subjective testing methods
- **Reference**
  - http://www.vqeg.org/

RECENT DEVELOPMENTS IN AUDIOVISUAL QUALITY ASSESSMENT AND MONITORING

Quality Assessment for Recognition Tasks (**QART**)

- **Mission**
  - *"To study effects of resolution, compression and network effects on quality of video used for recognition tasks"*
- **Goals**
  - To perform series of tests to study effects and interactions of
    - Compression
    - Scene characteristics
  - To test existing or develop new objective measurements that will predict results of subjective tests of visual intelligibility

Monitoring of Audio Visual Quality by Key Indicators (**MOAVI**)

- **Mission**
  - *"To collaboratively develop No-Reference models for monitoring audio-visual service quality"*
- **Goals**
  - To develop set of key indicators describing service quality in general
  - To select subsets for each potential application
  - To concentrate on models based on key indicators contrary to models predicting overall quality

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THANK YOU – QUESTIONS AND DISCUSSION

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Advanced multithreaded architectures for embedded microcontrollers

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Multithreaded architectures

- Nowadays processors can exploit many levels of parallelism:
  - Instruction-level parallelism (ILP)
  - Thread-level parallelism (TLP)
  - Memory-level parallelism (MLP)
- “Thread”
  - Explicit threads - defined by the programmer and managed by the operating system
  - Implicit threads - sequences of contiguous instructions (independent in comparison with other sequences), statically generated (by compiler) or dynamically generated (run-time by hardware)

Multithreaded architectures

- Explicit multithreading:
  - Interleaved Multithreading (IMT): the thread switching (context switching) is done by each pipeline cycle (each instruction) - fine grain multithreading;
  - Blocked Multithreading (BMT): the context switching is done by events that have long latencies (Load/Store instructions, RAW dependencies etc.) - coarse grain multithreading.
  - Simultaneous Multithreading (SMT): the concurrent issued instructions come either from the same thread, or from different threads.

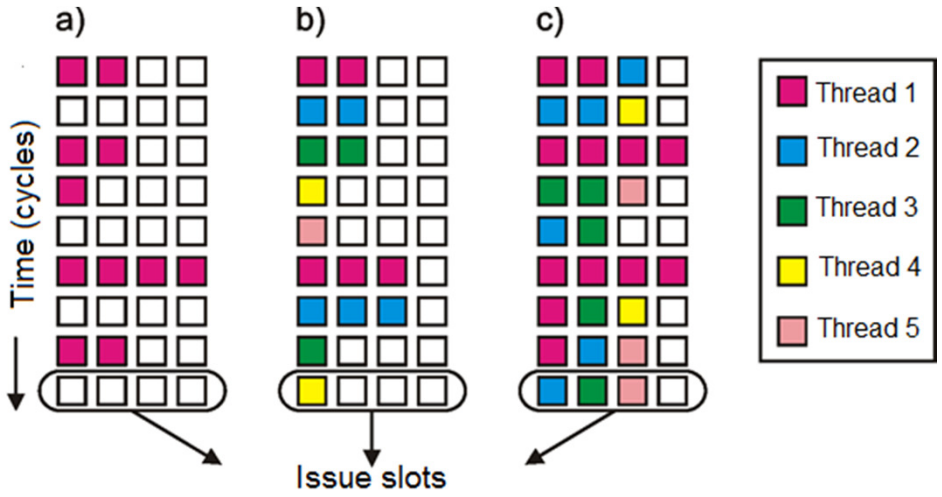


Figure 1. Context switching in: a) IMT b) BMT c) SMT processors.

Speculative multithreading

- Simultaneous Subordinate Microthreading

  (Chappell R.S., Stark J., Kim S.P., Reinhardt S.K., Patt Y.N., "Simultaneous Subordinate Microthreading (SSMT)", *Proceedings of the 26th Annual International Symposium on Computer Architecture*, 1999, pp. 186-195.)
- Minithreads Simultaneous Multithreading

  (Redstone J., Eggers S., Levy H., "Mini-threads: Increasing TLP on Small-Scale SMT Processors", *Proceedings of the 9th International Symposium on High Performance Computer Architecture (HPCA-9)*, 2003.)
- Hardware Scouting

  (S. Chaudry, P. Caprioli, S. Yip, M. Tremblay, "High performance throughput computing", IEEE Computer Society, 2005.)
- Inter-core Prefetching

  (Md Kamruzzaman, S. Swanson, D. M. Tullsen, "Inter-core prefetching for multicore processors using migrating helper threads", Proceedings of the sixteenth international conference on Architectural support for programming languages and operating systems (ASPLOS'11), 2011, pp. 393-404.)
- Etc.

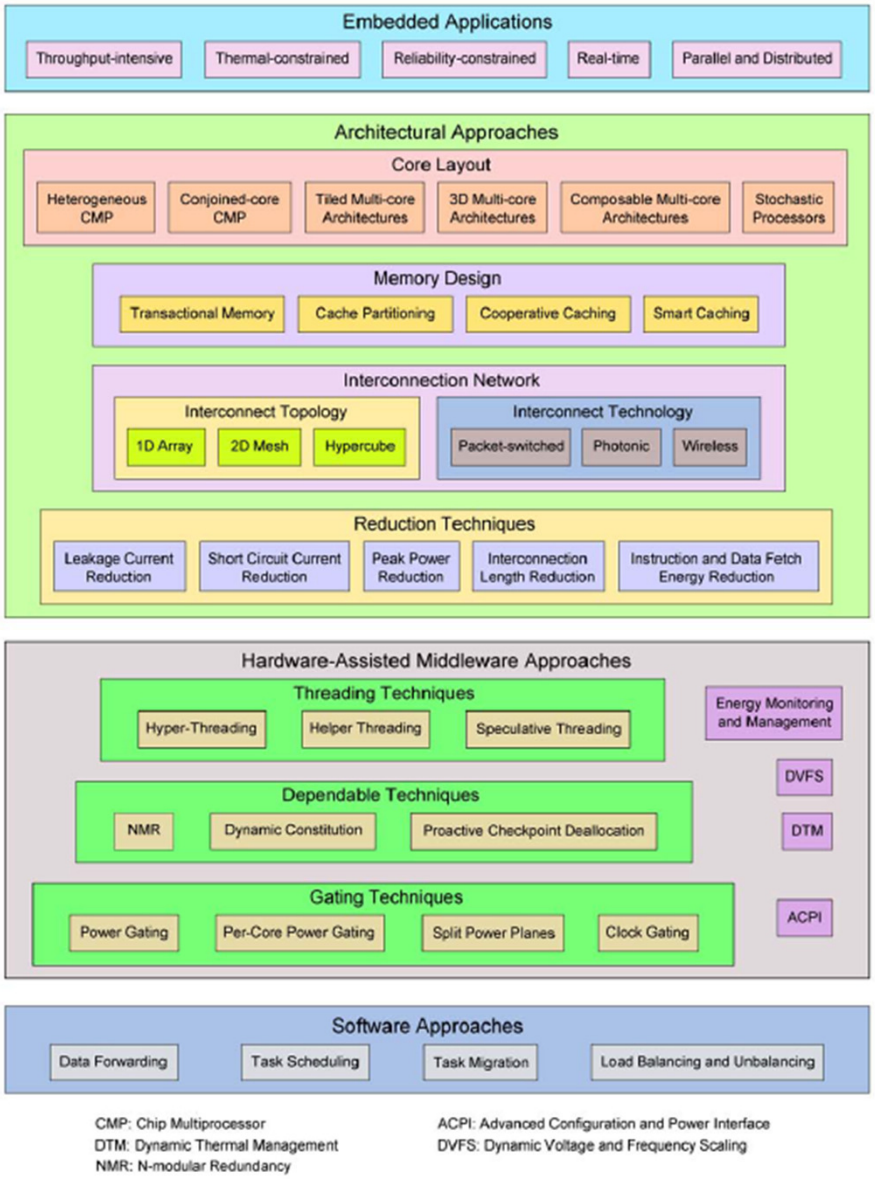
Multicore architectures

- The fraction of sequential code within the program limits the performance of parallel machines (the Amdahl law) [1] [9].
- The multicore architectures are built from superscalar and multithreaded processors.
- The multicore processors must manage fewer resources and be able to manage multiple tasks simultaneously.
- The performance of a multicore system is $\sqrt{n}$, where n is the number of cores [2].
- The embedded applications require the development of multicore processors that can be integrated into a smaller area like a classic microcontroller.

High-Performance Computing

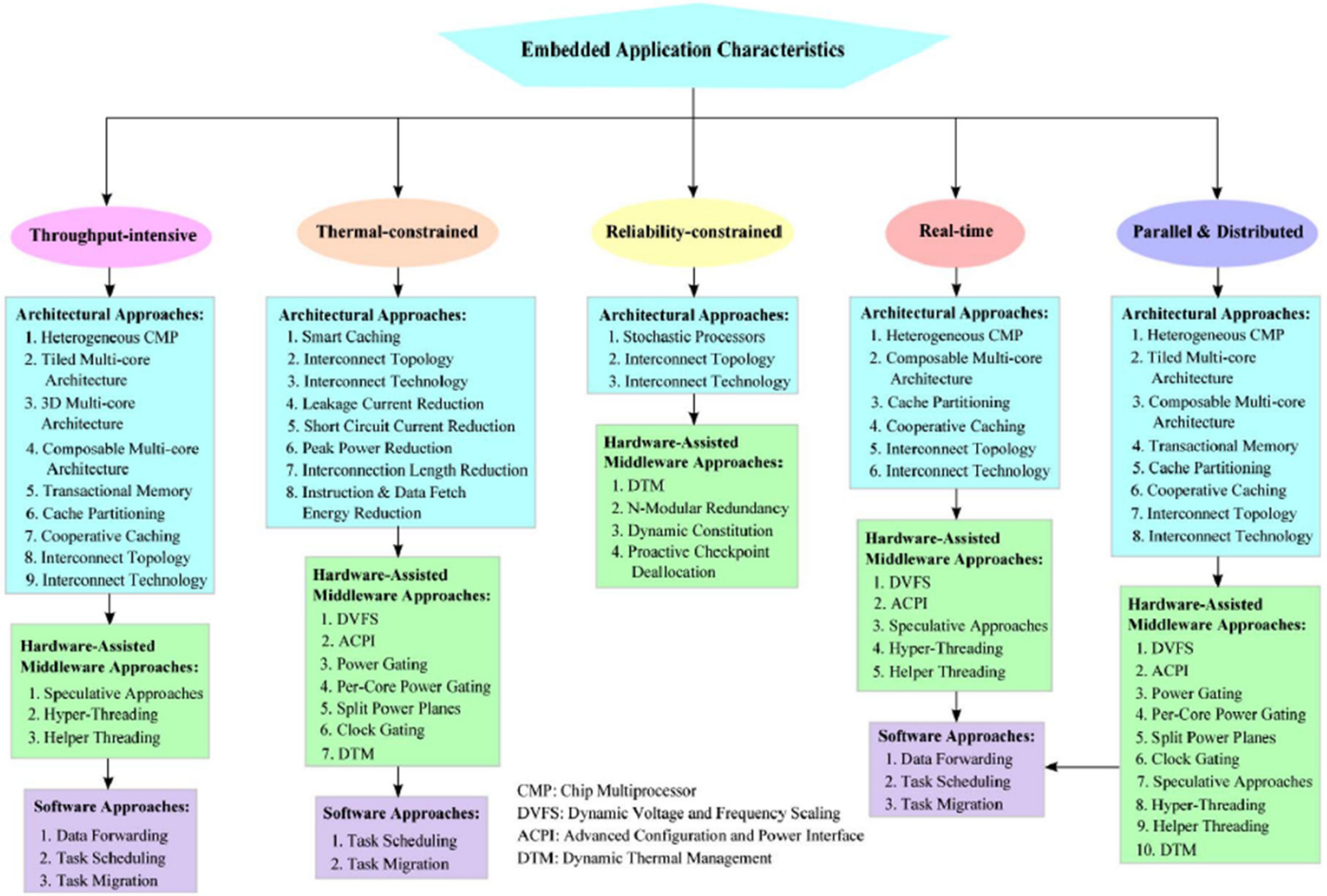
- High-Performance Computing (HPC) specify the applications that run on supercomputers.
- High-Performance Embedded Computing (HPEC) refers to the embedded applications that demand massive calculations.
- HPEC applications must comply with more stringent rules than HPC applications on supercomputers.
- High performance energy-efficient embedded computing applications (HPEEC) refers to the applications which are efficient in terms of energy consumption and performance.

HPEEC domain



A. Munir, S. Ranka, A. Gordon-Ross, “High Performance Energy Efficient Multicore Embedded Computing”, IEEE Transactions on Parallel and Distributed Systems, vol. 23, no. 4, 2012, pp. 684-700.

HPEEC domain



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Multicore/multithreaded processors

[TABLE 3] TABLE OF GENERAL-PURPOSE SERVER AND MOBILE/EMBEDDED MULTICORES.

	ISA	MICROARCHITECTURE	NUMBER OF CORES	CACHE	COHERENCE	INTERCONNECT	CONSISTENCY MODEL	MAX. POWER	FREQUENCY	OPS/CLOCK
AMD PHENOM [11], [15]	X86	THREE-WAY OUT-OF-ORDER SUPERSCALAR, 128-B SIMD	FOUR	64 KB IL1 AND DL1/ CORE, 256 KB L2/CORE, 2-6 MB L3	DIRECTORY	POINT TO POINT	PROCESSOR	140 W	2.5 GHZ–3.0 GHZ	12–48 OPS/ CLOCK
INTEL CORE I7 [2], [5]	X86	FOUR-WAY OUT-OF-ORDER, TWO-WAY SMT, 128-B SIMD	TWO TO EIGHT	32 KB IL1 AND DL1/ CORE, 256 KB L2/CORE, 8 MB L3	BROADCAST	POINT TO POINT	PROCESSOR	130 W	2.66 GHZ–3.33 GHZ	8–128 OPS/ CLOCK
SUN NIAGARA T2 [16], [17]	SPARC	TWO-WAY IN-ORDER, EIGHT-WAY SMT	EIGHT	16 KB IL1 AND 8 KB DL1/ CORE, 4 MB L2	DIRECTORY	CROSSBAR	TOTAL STORE ORDERING	60–123 W	900 MHZ–1.4 GHZ	16 OPS/CLOCK
INTEL ATOM [18], [5]	X86	TWO-WAY IN-ORDER, TWO-WAY SMT, 128-B SIMD	ONE TO TWO	32 KB IL1 AND DL1/ CORE, 512 KB L2/CORE	BROADCAST	BUS	PROCESSOR	2–8 W	800 MHZ–1.6 GHZ	2–16 OPS/ CLOCK
ARM CORTEX-A9‡ [6]	ARM	THREE-WAY OUT-OF-ORDER	ONE TO FOUR	(16,32,64) KB IL1 AND DL1/CORE, UP TO 2 MB L2	BROADCAST	BUS	WEAKLY ORDERED	1 W (NO CACHE)	N/A	3–12 OPS/ CLOCK
XMOS XS1-G4 [19]	XCORE	ONE-WAY IN-ORDER, EIGHT-WAY SMT	FOUR	64 KB LCL STORE/CORE	NONE	CROSSBAR	NONE	0.2 W	400 MHZ	4 OPS/CLOCK

‡Numbers are estimates because design is offered only as a customizable soft core.

[TABLE 5] TABLE OF DSP AND EXOTIC MULTICORES.

	ISA	MICROARCHITECTURE	NUMBER OF CORES	CACHE	COHERENCE	INTERCONNECT	CONSISTENCY MODEL	MAX. POWER	FREQUENCY	OPS/CLOCK
AMBRIC AM2045 [24], [25]	N/A	ONE-WAY IN-ORDER SR, THREE-WAY IN-ORDER SRD	168 SR, 168 SRD	21 KB LCL STORE/EIGHT CORES	NONE	NoC	NONE	6–16 W	350 MHZ	672 OPS/ CLOCK
ELEMENT CXI ECA–64 [26], [3]	N/A	ONE-WAY IN-ORDER, DATAFLOW CONNECTIONS TO 15 RECONFIGURABLE ALUs	FOUR CLUSTERS OF ONE CORE+ALUs	32 KB OF LCL STORE/ CLUSTER	NONE	HIERARCHIAL NoC	NONE	1 W	200 MHZ	64 OPS/CLOCK (16-B)
TI TMS320-DM6467 [14]	ARM, C64X	ONE ARM9 ONE-WAY IN-ORDER, ONE C64X EIGHT-WAY VLIW	TWO	ARM9: 16 KB IL1, 8 KB DL1; C64X: 32 KB IL1 AND DL1, 128 KB L2	NONE	BUS	WEAKLY ORDERED	3–5 W	ARM: 297–364 MHZ, C64X: 594–729 MHZ	1–9 OPS/ CLOCK
TI OMAP 4430 [12]	ARM, C64X	TWO ARM THREE-WAY OUT-OF-ORDER, ONE C64X EIGHT-WAY VLIW	THREE	N/A	BROADCAST AMONG ARM CORES	BUS	WEAKLY ORDERED	1 W	1GHZ	6–140 PS/ CLOCK
TILERA TILE64 [27], [28]	N/A	THREE-WAY VLIW	36–64	8 KB IL1 AND DL1/CORE, 64 KB L2/CORE	DIRECTORY	NoC	N/A	15–22 W	500–866 MHZ	108–192 OPS/ CLOCK
HIVEFLEX CSP2X00‡ [29]	N/A	TWO-WAY VLIW CONTROL CORE, FIVE-WAY VLIW COMPLEX CORE	TWO TO FIVE	2X CONFIGURABLE L1 FOR BASE CORE, LCL STORE FOR COMPLEX CORE	NONE	BUS	NONE	0.25 W	200 MHZ	2–22 OPS/ CLOCK

‡Numbers are estimates because design is offered only as a customizable soft core.

G. Blake, R.G. Dreslinski, T. Mudge, „A survey of multicore processors”, IEEE Signal Processing Magazine, November 2009, Vol. 26, Issue 6, pp. 26 – 37.

Conclusion

- Multithreading techniques are used in general purpose processors in order to increase their performances.
- Adapting these multithreading techniques on multicore/manycore processors lead to the increasing of the performance.
- This performance is gained through an efficient processing of the explicit threads.
- Speculative multithreading is used for the revealing of the hidden parallelism.
- A major challenge is the migration of this two forms of multithreading on embedded platforms.
- An important aspect, which we have not achieved in this presentation, is related to increasing the power consumption of the multithreaded processor, which has to be taken into account in evaluating its performance.

ACKNOWLEDGMENT

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PANEL EMERGING/AP2PS

Advanced Features in Emerging Systems and Technologies

Optical Network Bottom-up Organization Viability

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Outline

- Introduction
- Bottom-up organization proposal
- Results
- Challenges for discussion

Introduction

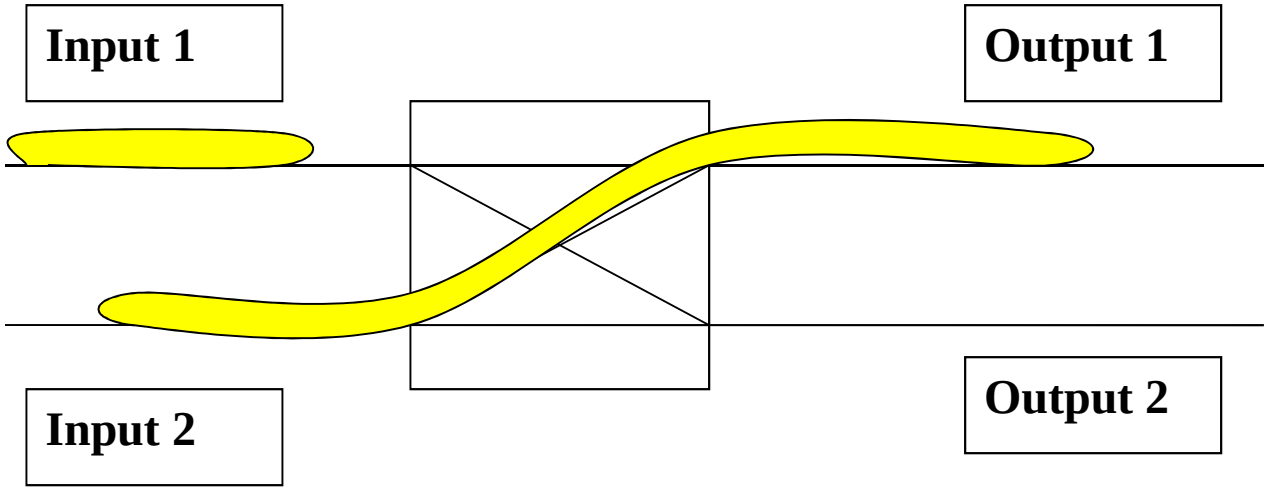
- The OPS (Optical Packet Switching) is an emerging technology since 30 years ago
- Now a days OPS has all the conditions to start to be applied to the metropolitan network: there are new photonic switching technology (including all optical logic devices) and there are demand for capacity and flexibility

Introduction

- Capacity is reported to be higher then 100 Tbps in a single optical fiber but that is not enough for the metropolitan area
- It is necessary Flexibility
  - to change the costumer ;
  - to change the technology;
  - to change the service type;
  - to change the capacity according to demands
- Packet switching can solve flexibility problem

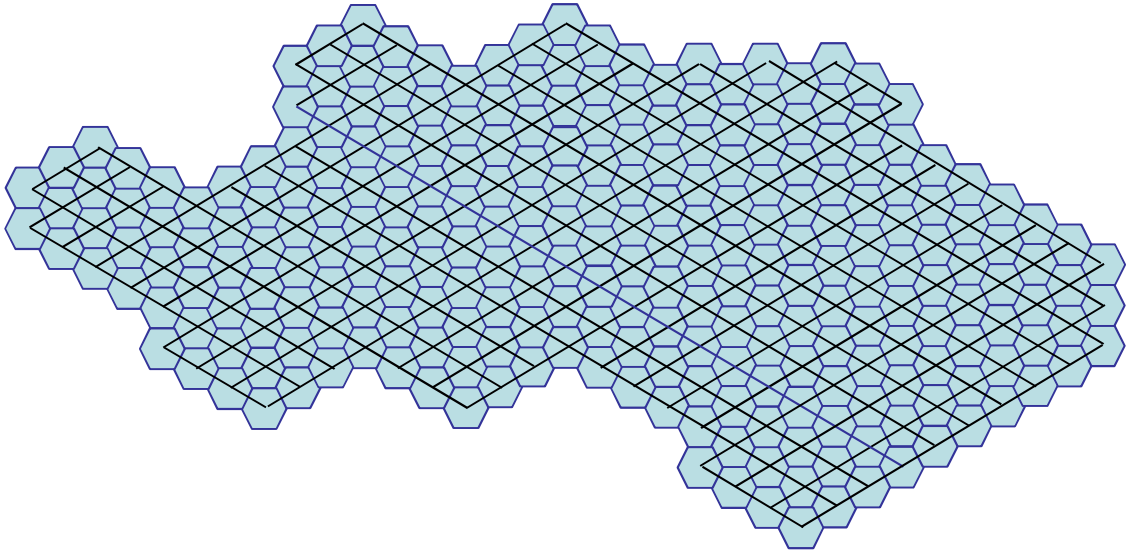
Bottom-up organization Proposal

- To simplify the photonic switching node removing optical buffers



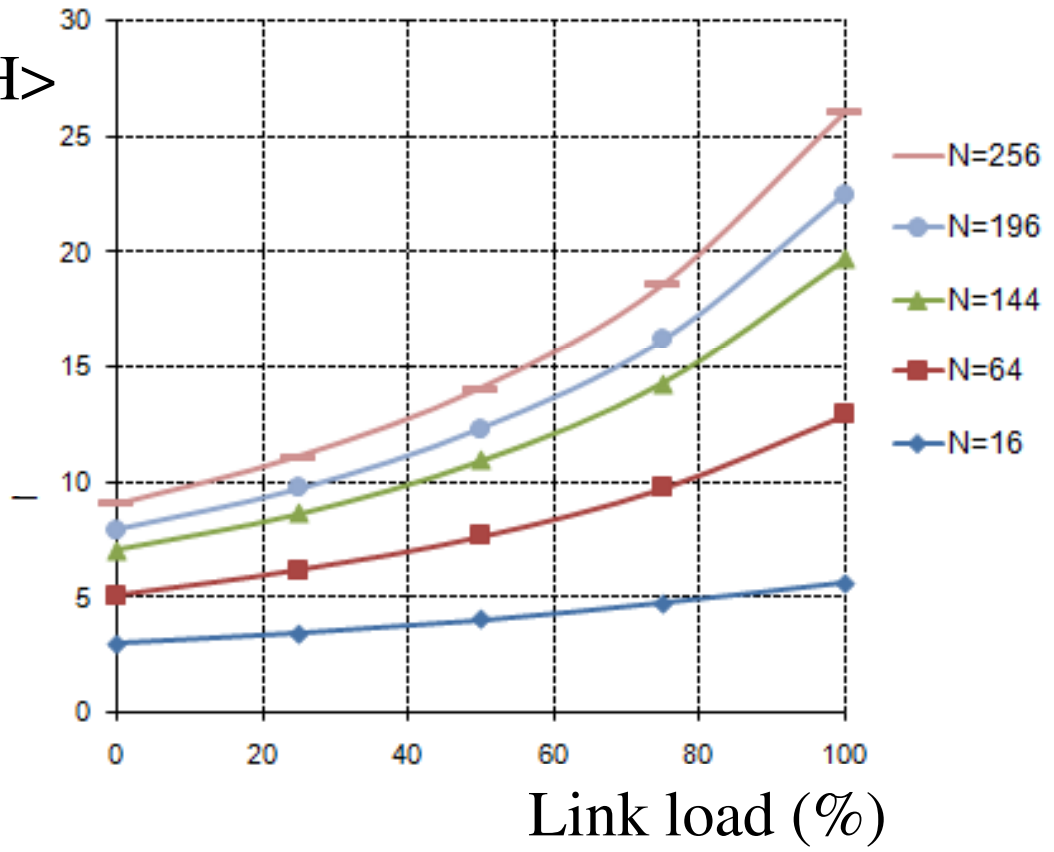
Bottom-up organization Proposal

- To treat the network as a complex system
  - switching operations can be performed by individual nodes using local information (bottom-up traffic organization)



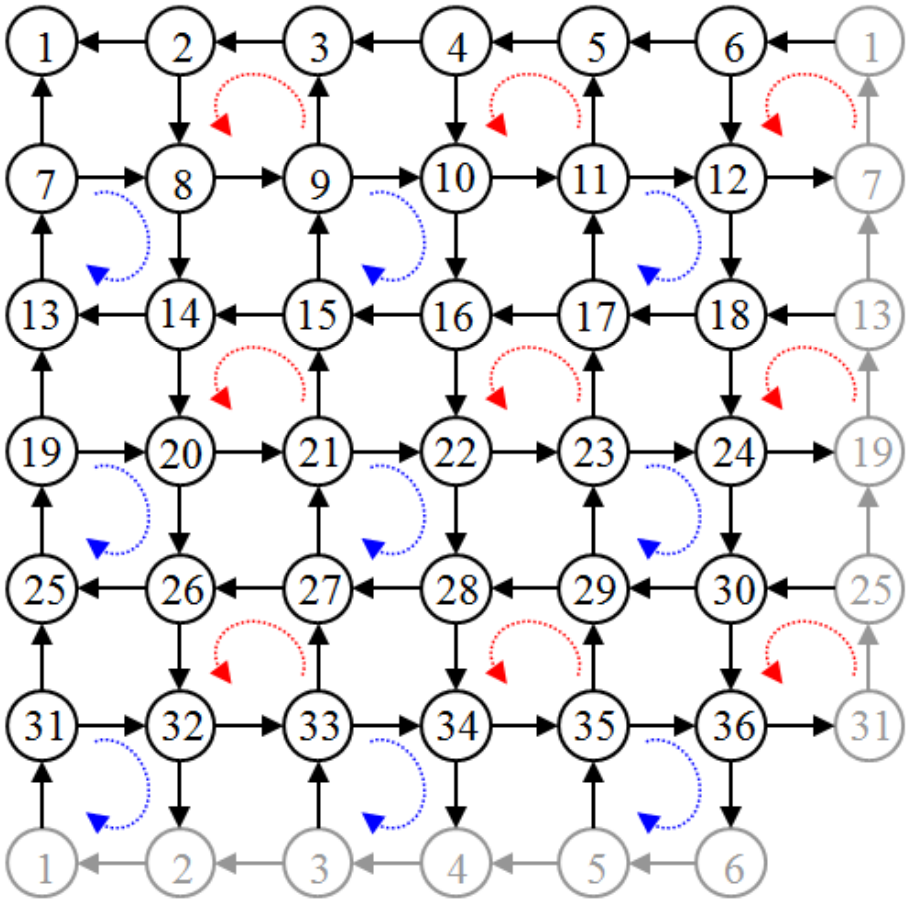
Results

- Performance evaluated by the mean number of hops <H> can be calculated by an statistical analytical model showing not to much higher <H> for large load condition



Results

- Protection can be implemented



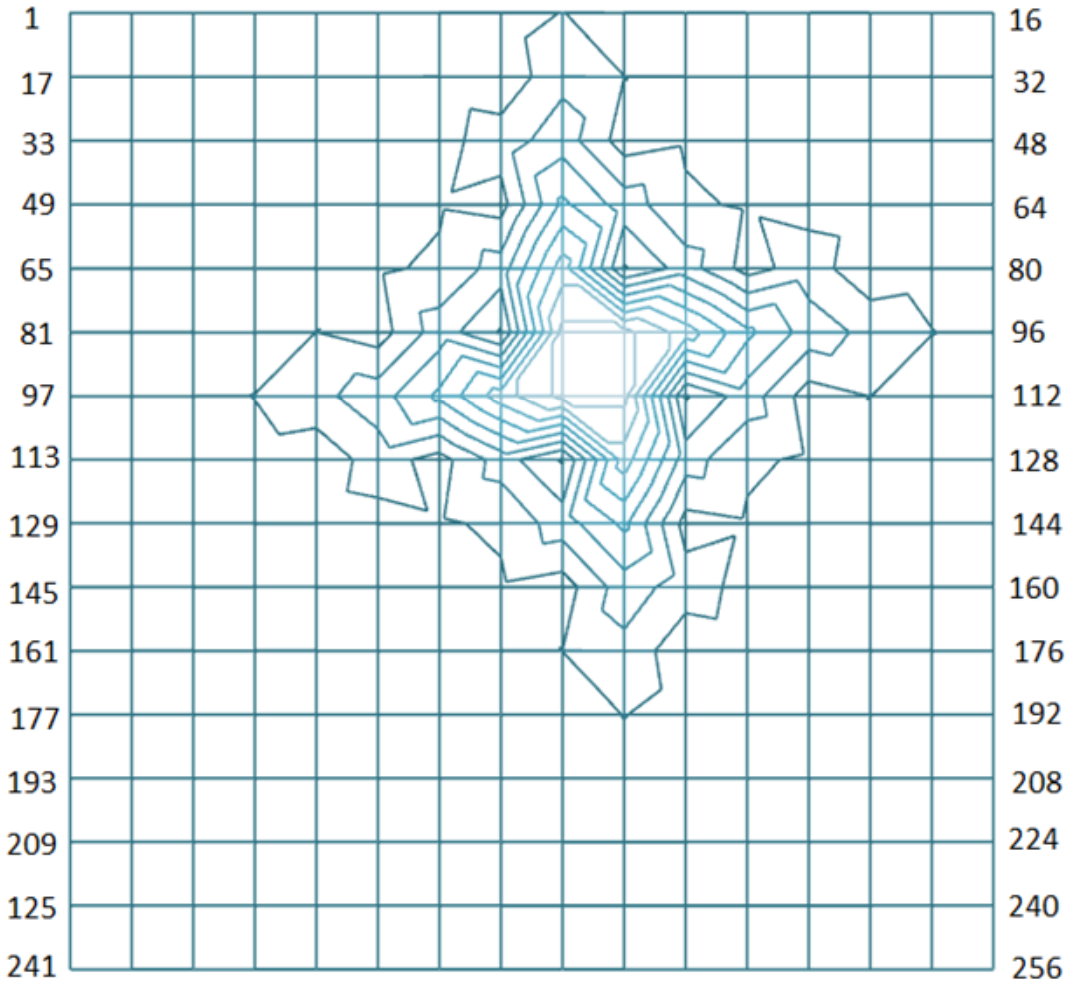
Anticlockwise: port 1 (Input 1 and Output 1)

Clockwise: port 2 (Input 2 and Output 2)

The sub-domain ring contains only 4 nodes

Results

- Failure segregation



Challenges for discussion

- **Future Work**

- Different topologies.
- Burst switching situation.
- Non-homogeneous traffic situation.
- Packet order mitigation.
- Packet loss consideration.
- Delay and delay variation.
- New Emerging Functions.
- Test bed construction.
- Other labs investigation.

Thank You Very Much

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